INSTRUCTION MANUAL

MODEL 2501

PROGRAMMABLE RGB COLOR
TEST PATTERN GENERATOR

A price for factory calibration from Phillis Becherich on JAN 26, 1989 was approx #200.00. Turn around time is usually less than 30 days.

INSTRUCTION MANUAL

MODEL 2501

PROGRAMMABLE RGB COLOR TEST PATTERN GENERATOR

Series H

April 19, 1985

Serial No. _____

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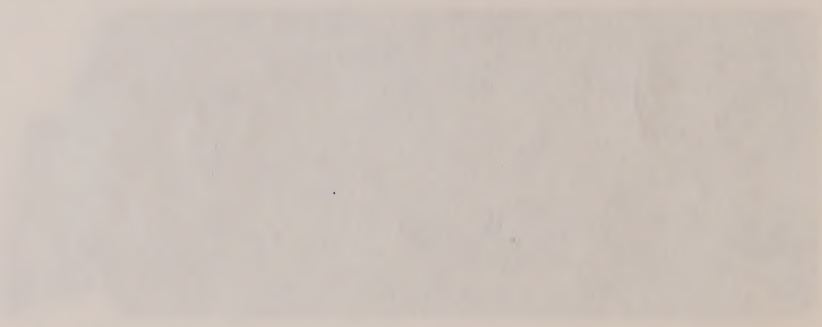

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Vii®

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NOTICE

This manual is prepared on the premise that the user is familiar with television system terms and concepts, and particularly is acquainted with the use of electronic test instruments (such as an oscilloscope) to interpret television waveforms and to relate the content of such waveforms to the pattern which would be produced on a typical television display device. If this is not the case, background reference material is suggested as follows:

a. Glasford, Glenn M., Fundamentals of Television Engineering (New York, NY: McGraw-Hill Book Co., Inc., 1955).

b. Showalter, Leonard C., Closed-Circuit TV for Engineers and Technicians (Indianapolis, IN: Howard W. Sams & Co., 1969).

c. Hansen, Gerald L., Introduction to Solid-State Television Systems (Englewood Cliffs, NJ: Prentice-Hall, Inc., 1969).

d. Fink, Donald G. (Ed.), Television Engineering Handbook (New York, NY: McGraw-Hill Book Co., Inc., 1957).

Please contact Visual Information Institute if additional information is desired on television tests and measurements or about application of this instrument.

You must read the instruction manual completely before connecting Vii test equipment for operation. Observance of a few procedures will provide greater operator convenience and will assure most effective application of the equipment as well as provide safety to the user.

(OVER)

CAUTION

Even low voltages commonly present in transistorized circuits are potentially dangerous. Additionally, full line voltage is present on fuse terminals, power switch terminals, and other exposed points within the interior of the unit, and are accessible when the cover of the equipment is removed. Caution should be exercised, as follows:

a. Remove power by unplugging the line cord when removing covers and inspecting interior of the unit.

b. Observe the common safety practices when servicing equipment (dry skin, insulation of the body from ground, etc.).

c. Never work on electrical equipment when alone. Service and calibration should be attempted only by a qualified electronics technician.

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INTRODUCTION

This instruction manual contains all essential information for the proper connection and use of Vii Test Equipment; this manual contains maintenance information as well.

This device contains circuits which are considered proprietary. Duplication of Vii Test Equipment is not authorized without the expressed, written consent of Visual Information Institute, Inc. These instruments, as described in this manual, are manufactured under U. S. Patent No. 3,483,479 plus other domestic and foreign patents pending.

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CAUTION

Even low voltages commonly present in transistorized circuits are potentially dangerous. Additionally, full line voltage is present on fuse terminals, power switch terminals, and other exposed points within the interior of the unit, and are accessible when the cover of the equipment is removed. Caution should be exercised, as follows:

a. Remove power by unplugging the line cord when removing covers and inspecting interior of the unit.

b. Observe the commonly safety practices when servicing equipment (dry skin, insulation of the body from ground, etc.).

c. Never work on electrical equipment when alone. Service and calibration should be attempted only by a qualified electronics technician.

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UNIVERSAL TIME BASE
FOR RASTER SCAN DISPLAYS

There is, literally, no order to the time base structure being employed in raster scan display devices used with computers and other digital equipment. Clock rates vary from less than 10 mHz to more than 80 mHz. Pixels per line vary from less than 250 to more than 1024. Synchronizing pulses may be described in terms of either pixels or time; often pulse widths are described in time to the third or fourth decimal place.

The diversity of rates and pixel/pulse structures presents a considerable challenge in developing equipment which can be universally applied to this broad range of systems. Measurement to such precision is substantially impractical to confirm proper raster structure.

In order to simplify equipment and calibration procedures, and thereby minimize equipment cost, Vii has developed a universal format for horizontal rate raster development based upon a 0.1 usec. (100 nsec.) timing increment. In this system, all horizontal rate parameters - e.g. Total H Line Time, H Blanking Width, H Front Porch, etc. - are programmed to the nearest 0.1 usec. For example, a horizontal line time calculated to be 38.096 usec. (for the 875/60 scan rate) would be rounded to 38.1 usec. The timing difference is minute; the only difference observed would be a slight change in vertical field time. In this example the slightly increased line time would make the vertical field time 16,668.75 usec. (59.9925 Hz vertical field rate) rather than the literal 16,666.66 usec. of a 60 Hz field rate.

Vertical parameters are established in increments of half lines. This conforms to long standing common practice to avoid scanning aberrations which may develop from vertical pulses that are not an integer of horizontal line structure. Raster structure is, universally, based on an even number of scan lines in two fields for non-interlaced scan and an odd number in two fields for 2:1 interlaced systems. Pulses, such as V Blanking, V Drive, V Front Porch and V Sync are configured to the nearest halfline. That is, if V Blanking were specified to be 698 usec. in the example 875/60 scan rate, it would equate to 18.320209 lines, which violates common practice. In the Vii standard system this would be rounded to 18 lines, resulting in 685.8 usec. V Blanking pulse width.

The minute differences outlined will not be of consequence in nearly all applications. If the shift of vertical field rate is significant due to hum or other effects, the 20 mHz master clock rate can be shifted slightly by use of an external clock slightly off 20 mHz.

Acceptance of the slight deviations as described greatly simplifies the design, construction and programming requirements for the raster scan systems. Another advantage is that all scan rates within design operating range can be matched, unlike gaps which are implied in a digital synthesizer system.

While long term common practice and U.S. standards (EIA Standards RS-170, RS-330 and RS-343) have been consistent in the timing of vertical sync interval, deviations have appeared. The Vii standard is consistent with common practice and U.S. standards:

V Front Porch = 3 lines

V Sync = 3 lines

V Post Equalizing = 3 lines

Serrations @ 2H rate

Equalizing pulses @ 2H rate

The leading and trailing edges of V Blanking and V Drive are coincident with the timing of the leading edge of H Blanking. The leading and trailing edges of V Sync are coincident with timing of the leading edge of H Sync.

Should there be an application which demands absolute timing conformance, the universal time base system may not apply. However, these applications can be satisfied with a customized system dedicated to that particular use. A technical note is available from Vii, "Structure of the Television Raster", which is a thorough discussion of all factors that influence structure and timing of the raster scan technique.

APPLICATIONS

The Model 2501 Programmable Test Pattern Generator develops precise synchronizing pulses for exact and effective synchronization of closed circuit television devices, including test pattern generators, cameras, display devices, etc.

This instrument is programmable by the operator for any scanning rate, including "standard" 525, 675, 729, 875, 945, 1023, 1029 and 1225/60 Hz field rates and 625/50 Hz field rate, all 2:1 interlace; these rates and other "non-standard" line numbers may be employed by selection of the proper horizontal line time and scan lines per field by keypad entry. The generator develops an interlaced (2:1) television raster or non-interlace (1:1) condition automatically through selection of the number of scan lines in two fields, also entered by keypad.

Horizontal sync and pattern parameters are entered in timing increments of 0.1 usec; vertical parameters are entered in increments of 0.5 t.v. lines. It is designed for use with horizontal line times of from 10 usec. to 204 usec. and up to 2048 lines per display field. The Model 2501 allows the user to build a rate, each parameter at a time, or to choose standard proportion and format which will be computed automatically. Rates may be stored, recalled for use, edited or deleted by keypad entries. Software "lockout" is provided to prevent unauthorized editing without proper security password.

This particular generator can provide synchronizing waveforms as specified by Electronic Industries Association Standards RS-170, RS-330 and RS-343. In addition to the H Drive, V Drive and mixed Blanking, this unit generates a composite Sync signal. The Sync signal can include front porch delays in the vertical and horizontal sync and serrations and equalizing pulses in the vertical sync interval in accordance with NTSC convention. Sync format can be programmed in any one of six modes, Broadcast, Industrial, Military, and three custom modes. Broadcast, Industrial and Military sync formats have V front porch, V sync, and V post equalizing intervals fixed at three lines each. These parameters may be programmed as desired for custom modes, limited only by vertical field length.

Change of scan rate and pulse format is readily accomplished in this generator as explained in the DESCRIPTION OF A SCAN RATE section (page 65).

Television test patterns developed by the Model 2501 are employed primarily in the alignment and performance analysis of closed-circuit and studio television equipment. Generally alignment is performed in conjunction with test charts developed by Vii. Further information regarding television tests and measurements is available through Visual Information Institute, Inc.

Vii test equipment is designed to be used with television systems (those which do not place the video signal upon an r-f carrier), including those with rates as set forth by EIA Standards RS-170, RS-330, RS-343 and RS-375 (from 525 to 1023-line) as well as European 625-line, 50 cycle and other specialized systems such as 64 kHz, etc. It is necessary only to program the generator to develop the scanning rate desired at any particular time.

The programmable sync generator section produces outputs in conventional Video format, or TTL level pulses. The Video format produces H Drive, V Drive, Blanking and Sync, each one at 4.0v. pk-pk level, a.c. coupled, negative going pulses when properly terminated in a 75 ohm coaxial cable. The TTL level pulses, H Trigger, V Trigger, Blanking, composite Sync, H Sync and V Sync may be selected as either positive or negative going pulses, are direct coupled, and are driven out by a TTL pulse driver at a nominal 75 ohm source impedance at a nominal 1.8v. terminated and +4.0v. $\pm$0.7v. unterminated. The H Trigger and V Trigger leading edges may be varied with respect to time of the leading edges of Blanking to position alpha-numeric information on the display screen as desired.

The Model 2501 develops complete video signals that will generate the display of precise patterns as selected in both the conventional Video signal format and in TTL compatible format. Separate outputs are provided on the rear panel for each mode.

The nominal output levels in conventional Video are 1.0v. video (including blanking pedestal), plus 0.4v. sync to develop a 1.4v. pk-pk composite video signal. The output may be adjusted to supply a 1.0v. composite signal of 0.786v. plus a 0.214v. sync. Keypad entry permits operation with a non-composite output (no sync) if desired. The generator is source terminated for proper drive of 75 ohm coaxial line, direct coupled.

The TTL format produces video only (no pedestal or sync added) at a nominal 10 nsec. rise and fall time, direct coupled, at a +4.0v. $\pm$0.7v. level when unterminated, or at a 1.8v. level when terminated. This output has a nominal 75 ohm source impedance.

Vii test equipment produce exceptionally sharp risetimes, 10 nsec. for the Video and TTL formats. Many systems and components generate distortion when sharp transitions are introduced. Units are provided from the factory with risetime unlimited unless otherwise specified. The TTL VIDEO circuit card may be modified to decrease output signal risetime as desired for any particular application; contact the factory for additional information.

Resolution modulation depth is directly related to the bandwidth and risetime capabilities of the system. Vii test instruments are designed to provide full, 100% modulation to quite high resolution content. However, at higher rates a roll-off may be evident as limited by risetime. Also short lengths of coaxial cable will load high frequency information, reducing the modulation level to less than full black-to-white excursion.

This instrument develops test signals on three individual video channels (red, green and blue) for the RGB, three cable color system format (not encoded with 3.579545 mHz subcarrier). Each of the test patterns is described in detail in the following text.

The Model 2501 can provide a composite video signal on any or all of the three video outputs. A common system configuration is to have a composite video signal on the green channel, and a non-composite signal on the red and blue channels by adjustment of sync level to zero on these channels. The user can select a Non-composite or Video Only signal on all three output channels by circuit card control.

A primary use of the Model 2501 is evaluation of scan linearity and geometry of a display monitor, using the Bars or Dots patterns. It is common practice to make such evaluation by comparing the displayed pattern to a reference linearity chart projected onto the display surface. Technical Notes and Charts are available from Vii; please contact the factory for further information.

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TECHNICAL SPECIFICATIONS

This specification defines the characteristics of a multiple scan rate test pattern generator for raster scan display devices operating in the range of from 10 kHz to 100 kHz horizontal repetition rate at various numbers of scan lines per field and vertical field rates. Horizontal sync and pattern parameters may be entered by keypad in 0.1 usec. timing increments; vertical parameters are entered in increments of 0.5 t.v. lines. Non-volatile storage is provided for up to 69 separate raster structures. Parameters and timing are indicated on a 16 segment alpha-numeric display. The operator may build a rate, each parameter at a time, or may choose standard proportion and format which will be computed automatically. Rates may be stored, recalled for use, edited, or deleted by keypad code entries. Software "lockout" is provided to prevent unauthorized editing without proper security password. A basic set of test patterns is provided for thorough evaluation of television raster type display devices.

Raster Structure

Established by keypad entry of individual timing parameters for each raster desired, in the range of 10 kHz to 100 kHz horizontal rate:

Horizontal Parameters (0.1 usec. timing increments):
- Total H Line Time
- H Blanking
- H Front Porch
- H Sync
- 2H Serrations
- 2H Equalizing
- H Drive
- H Trigger Phase
- H Trigger Width

Vertical Parameters (1/2 line timing increments):
- Scan Lines in Two Fields
- V Blanking
- V Front Porch (V Trigger Phase)
- V Sync (V Trigger Width)
- V Trigger Phase
- Sync Format

Test Patterns

Horizontal proportion is clocked from 20H rate unless non-standard entry is desired on allowed patterns. Selections available through keypad entry include:

Horizontal Pattern Proportion (0.1 usec. increment):
- V Bar Position
- V Bar Spacing
- H Window Start
- H Window Stop

Vertical Pattern Proportion (scan line in active field):
- H Bar Position
- H Bar Spacing
- V Window Start
- V Window Stop

Storage

Up to 69 separate rasters, access by two digit code.

Test Pattern Functions

Flat Field . . . . Uniform level over entire raster area, at 50% gray level (50% APL),or 100% white level.

Bars . . . . . As programmed, nominal 17 V Bars and 14 H Bars to form a grid ("crosshatch" or "grating") for linearity reference in both display planes simultaneously.

Dots . . . . . Small points developed at the intersections of H Bar and V Bar elements, especially for measurements with linearity charts.

Gray Scale . . . . Standard ten level, slope adjustable to linear or log.

Window . . . . . As programmed, nominal 25% duty cycle (25% APL) for combined transient and low frequency response tests.

V Stripe . . . . . Nominally 50% of each t.v. line at white level, 50% black level for test of transient and mid-frequency response.

Color Bars . . . . An eight segment color pattern of NTSC format to evaluate fidelity of color video displays.

Scan Rates

This instrument is programmed by the operator for use at any scan rate, including "standard" 525, 675, 729, 875, 945, 1023, and 1225/60 Hz field rates and 625/50 Hz field rate, all 2:1 interlace; these rates and other "non-standard" line numbers may be employed by selection of the proper horizontal line time and scan lines per field by keypad entry. It is designed for use with horizontal line times of from 10 to 100 usec., and up to 2048 lines per display field.

Power Requirements

Voltage	120v. (105 to 135v.) a.c. - or - 220v. (200 to 270v.) a.c. - or - 240v. (200 to 270v.) a.c.
Current	Approximately 1½ amp at 120v.
Power	Approximately 150 watts.
Frequency . . .	50/60 Hz.
Fuse Rating . .	2 amp slo-blo.

Mechanical Characteristics

Enclosure . . .	Cabinet for bench top use. Optional rack slides available.
Cabinet Size .	7" high x 17" wide x 20" deep (18cm high x 43cm wide x 51cm deep).
Weight	Approximately 36 lbs (16.3 Kg).
Temperature . .	0 degrees C to +55 degrees C.
Humidity . . .	Up to 95%.
Connectors . .	BNC series.
Rack Mount . .	Rack mounting kit with chassis slides available for standard 19" electronic equipment cabinets (Model RMS-24).

NOTE: In the interest of product improvement, these specifications are subject to change without notice.

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Resolution . . . Square wave bar pattern at selected repetition rate to maximum of 30 mHz to develop desired "resolution t.v. lines" in five increments at full, 100% black-to-white contrast. Presented as continuous, or in bursts with selectable reference bars.

Video . . . . . A combination test pattern that includes:
Resolution - five bursts in the left half of the display.
Black Reference - segments of whiter-than-black, black and blacker-than-black, at the center of the display.
Gray Scale - standard ten step, linear staircase, including black, white, and eight intermediate shades of gray occupy right half of the display.

Combination . . Contains in one raster simultaneously the Video pattern plus Color Bars.

Character . . . Development of a block "C" with a small "x" superimposed to form rows across the television display screen. Characters are in a 5 x 7 pixel format, seven scan lines tall. Rows are separated by three inactive scanning lines. The number is adjustable, nominally 40 to 80 characters per row, depending upon scan rate, to a maximum 25 mHz clock rate.

Output Signals - Test Pattern Generator Section

Three individual video channels for red, green and blue components of an RGB color television system.

Video Format

Type . . . . Composite video.

Level . . . . Video - adjustable 0 to 1.0v., internal control.
Blanking - adjustble 0 to 0.125v. internal control.
Sync - adjustable 0 to 0.4v. internal control.

Impedance . . 75 ohm, source terminated.

Risetime . . 10 nsec. nominal rise and fall time in video portion of signal.

Coupling . . D.C. (direct coupled).

Polarity . . White positive, sync negative.

Connectors . BNC type coaxial.

Output Signals - Test Pattern Generator Section (cont.)

TTL Video Format

Type	Video only, without blanking "setup" or sync.
Level	TTL compatible, nominal +4.0v. ±0.7v. unterminated.
Impedance . .	Nominal 75 ohms source terminated.
Coupling . .	D.C. (direct coupled).
Polarity . .	White positive.
Risetime . .	Nominal 10 nsec. rise and fall times.

Output Signals - Programmable Sync Generator Section

Video Format

Type	H Drive, V Drive, Blanking, Sync.
Level	4v. pk-pk nominal when terminated.
Impedance . .	Nominal 75 ohm source termination.
Coupling . .	D.C. (direct coupled).
Polarity . .	Negative-going pulses.
Risetime . .	Nominal 100 nsec.

TTL Format

Type	H Trigger, V Trigger, Blanking, Sync, H Sync, V Sync.
Level	TTL compatible, nominal +4.0v. ±0.7v. unterminated.
Polarity . .	Individually selectable at rear panel for each function, negative-going or positive-going pulse.
Impedance . .	Nominal 75 ohm source terminated, from TTL driver.
Coupling . .	D.C. (direct coupled).
Risetime . .	Nominal 50 nsec.

INSTALLATION

Please read the instruction manual completely before connecting Vii test equipment for operation. Observance of only a few procedures will provide greater operator convenience and will assure most effective application of the equipment as well as provide maximum safety to the user.

The basic cabinet is provided with four feet so that the instrument may be employed as a free-standing bench instrument, in which case the unit is ready for use as unpacked. Addition of the chassis slide accessory kit permits installation of the unit into a standard 19" equipment rack of proper depth on slides to permit front "drawer" access to the equipment. In such installations, observe precautions on temperature and cooling air.

Prior to initial operation, establish that all circuit cards are placed into their proper position, and that they are firmly seated into the connector.

* *

CAUTION

BE SURE THAT PROPER POWER SELECTION IS MADE BEFORE PLUGGING IN THE POWER CORD. APPLICATION OF IMPROPER POWER WILL RESULT IN DAMAGE TO THE INSTRUMENT AND WILL VOID THE WARRANTY.

* *

The instrument must be provided with an appropriate supply of alternating current; the dual voltage input may be configured for operation at 120v., 220v. or 240v. by position of the printed card insert behind the fuse in the rear panel power cord receptacle. Remove the fuse, and slide the insert into the recess with the voltage desired up and facing the operator. Replace the fuse. It is strongly recommended that three-wire single phase wiring (one wire grounded) be employed for maximum safety to personnel operating this or other types of electronic equipment.

The letter "S" in the model number indicates a major special feature has been made to the instrument per customer specification. The letter "M" in the model number indicates that a minor modification has been made to the instrument to customer specification. Detail of the changes will be described in the MODIFICATIONS section of this manual.

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CONNECTIONS

Power is applied to the Model 2501 by inserting the line cord into an a.c. receptacle of proper voltage and frequency, and turning the power switch on. The red pilot light indicates that power is applied and the unit is ready for operation. Figure 1 (page 19) illustrates a typical installation for test of a television display device.

This instrument contains an internal sync generator; no inputs are required and the rear panel connectors will serve as auxiliary sync outputs for external use. These outputs should be terminated if pulses are not used elsewhere.

COMPOSITE VIDEO OUTPUT	Of variable amplitude signal portion, fixed level of blanking and sync (internaly adjusted). These signals should be routed through coaxial cable of proper characteristic impedance to the point of utilization.
TTL VIDEO OUTPUT .	The signal should be routed through coaxial cable of proper type and impedance to the point of utilization. This signal should be routed over a short cable run to avoid risetime degradation. If not used, this output should be terminated to avoid signal radiation.

* *

ALL COAXIAL CABLES SHOULD BE TERMINATED PROPERLY.

ALL UNUSED OUTPUTS SHOULD BE TERMINATED AT THE REAR PANEL. Operation with unused outputs not terminated may cause crosstalk between outputs.

* *

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FRONT PANEL CONTROLS

POWER ON-OFF . . . Main switch to control application of a.c. power to the unit.

FUNCTION SELECT . Selector switch which permits the operator to choose the function developed in the video output signal.

RESOLUTION SELECT . When main Function Selector is in the RESOLUTION position, this switch permits selection of Resolution Repetition Rate that is in use.

DOT WIDTH . . . . . Potentiometer control to adjust size of vertical bar elements in the Bars pattern and width of dot elements in the Dots pattern.

PROGRAMMABLE SYNC GENERATOR . . Keypad and related controls for entry of individual timing and pattern parameters for each raster desired with horizontal parameters in 0.1 usec. timing increments, and vertical parameters in half-line increments. Operation of this module is fully described in the DESCRIPTION OF A SCAN RATE (page 65) section.

TEST POINTS . . . To verify presence of proper H Drive, V Drive, Blanking, Sync and Video Output signals at the inputs and outputs.

NOTE: Video test points on the front panel are used only to verify presence of signal. They are isolated from the actual rear panel outputs and do not indicate true quality of the signal. They are intended for use with a high impedance probe only.

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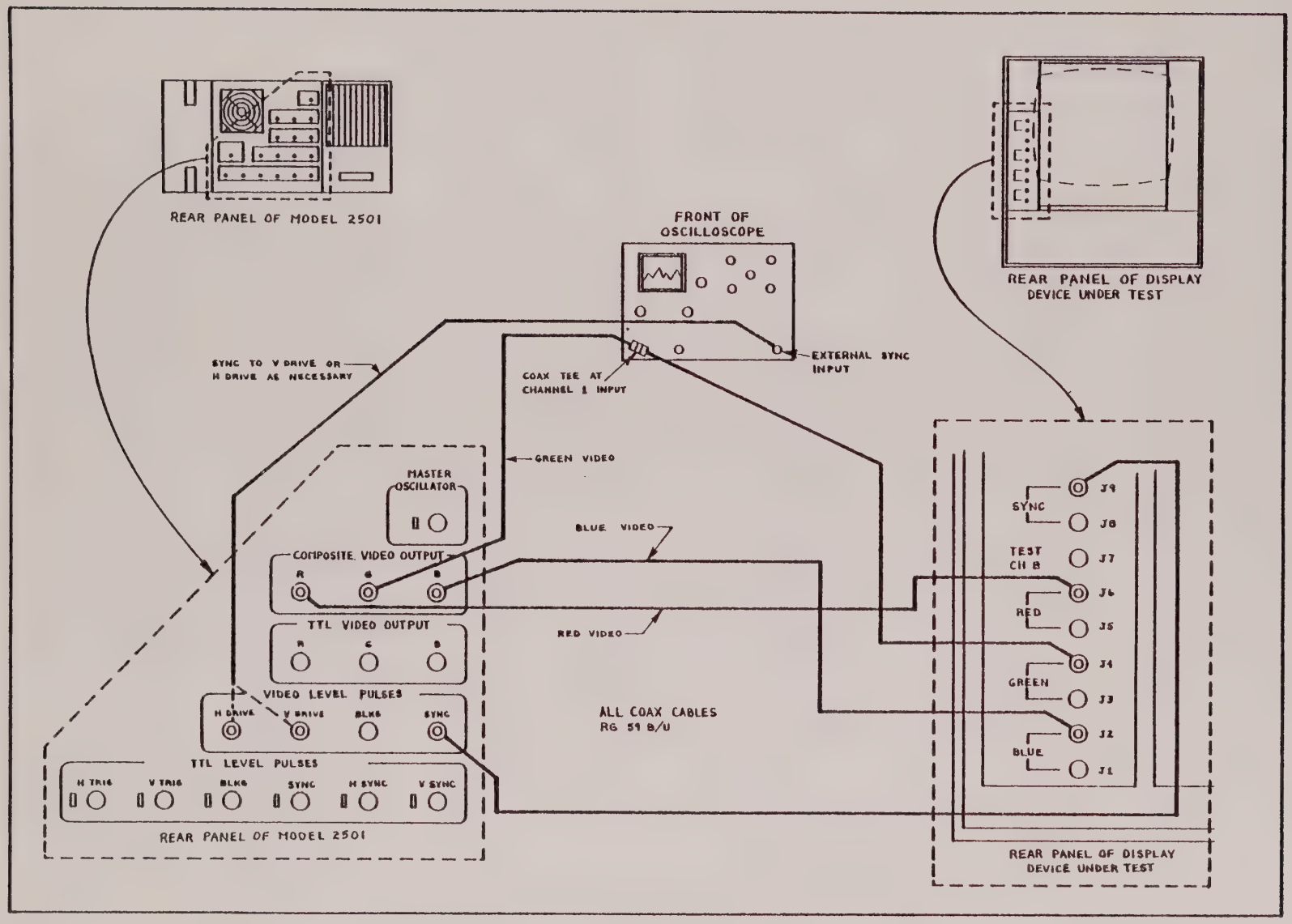

Figure 1 - Typical Test Setup

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OPTIONS IN OPERATION

The user has a choice of different operating conditions in this instrument. Selection should be made depending upon equipment and testing requirements.

SCAN RATE AND INTERLACE RATIO . . . . The generator may be operated at various scan rates, either at 2:1 interlace or 1:1 non-interlace, as programmed. Rate is chosen by keypad entry of raster parameter, as outlined in PROGRAMMING AND USER CODES (page 75). Selection of an odd number of scan lines will produce a 2:1 interlaced raster. Selection of an even number of scan lines will produce a 1:1 non-interlaced raster. Refer to DESCRIPTION OF A SCAN RATE (page 65) for further information. The range which operation is possible is described in PROGRAMMING RANGES (page 71).

VIDEO OUTPUT FORMAT . . . . While all three video outputs (red, green and blue) may be composite, usually the green channel video signal is composite, while the red and blue channels may be non-composite by reducing the sync level to zero. The green signal can be made non-composite by circuit card adjustment; this adjustment should be performed as described in PERFORMANCE VERIFICATION (page 93). If all three video signals are non-composite, the equipment under test should be synchronized externally with the H Drive and V Drive signals, Sync or other appropriate pulse outputs.

SYNC FORMAT. . . . The composite sync signal (including the sync portion of the green channel composite video signal) may be programmed in one of six modes - Broadcast, Military, Industrial, or one of three custom modes. They are explained fully in DESCRIPTION OF A SCAN RATE (page 65).

TTL PULSE POLARITY . . . . The TTL format pulses from the sync generator section may be of either positive or negative polarity, individually selected by switches on the rear panel. The TTL PULSE OUTPUT card (L-2118) can provide any one of three types of TTL compatible outputs depending upon the application:

a. The 74128 line driver is provided, unless otherwise specified, with source termination resistance of 75 ohms. This configuration is optimum for driving long lengths of coaxial cable, providing 2v. pk-pk of signal when cable is terminated, 4v. pk-pk with an unterminated line. Signal level may be increased by replacing source terminating resistors R44, R45, R46, R47, R48 and R49 by a jumper. Source impedance then will be approximately 20 ohms providing a 3v. pk-pk signal with terminated cable.

b. The 7428 buffer may be substituted for the 74128 line driver. This provides a standard TTL gate output with nominal 4v. pk-pk signal. This configuration is suitable for driving equipment with TTL gate inputs, but is not recommended for long cable runs.

c. The 7433 open collector buffers may be substituted for the 74128 line driver. This configuration is suitable for use with equipment which has TTL gate inputs with a collector load connected to +5v. Use caution when using this configuration; be sure grounds are connected between units and that connections are made with the power off in both pieces of equipment being interconnected. This output is not recommended for long cable runs.

VIDEO LEVEL CALIBRATION . . . . This instrument has been configured at the factory (unless otherwise specified) for a maximum of 1.0v. composite video signal (0.714v. video + 0.286v. sync) on all three (Red, Green and Blue) video channels. Signal level maximum may be extended to 1.4v. composite video (1.0v. video + 0.4v. sync) by removing resistor R38 from each of the TTL VIDEO circuit cards (Positions 3C, 4C and 5C). A slight trimming adjustment of video and sync levels may be required to obtain exactly 1.4v. composite video.

FLAT FIELD 50%/100% LEVEL . . . This instrument is designed to provide 50% gray level in the Flat Field function. Some applications require the Flat Field level to be 100% white. This can be obtained by removing the specified jumper from the GRAY SCALE circuit card (4000, Position 4B). Refer to drawing L-4000 (GRAY SCALE) at the rear of this manual.

OPERATION

Power is applied to the instrument by inserting the line cord into an appropriate power source, 120v. a.c. at 50/60 Hz. The instrument is turned ON by the power switch at the right side of the front panel. The pilot light on the front panel will indicate that power is applied to the instrument. When power is applied to the unit, RATE 99 525/60.0 will be displayed. (This default scan rate is permanently programmed and cannot be altered. The instrument will return to this rate whenever power is interrupted.) If this procedure is followed and the red pilot light is not on and RATE 99 is not displayed, it would indicate that either power is not applied to the instrument or that the instrument fuse is blown. The fuse is located at the rear panel power input connector assembly. If defective, the fuse should be replaced with one of proper rating as set forth in TECHNICAL SPECIFICATIONS (page 9). If the fuse is not defective and the instrument still is not operable, the source of power should be verified.

If the pilot light indicates that power is applied and all connections have been made, yet the RATE 99 is not displayed, this indicates that the sync generator computer requires service. Or if the pilot light is ON and RATE 99 is displayed, yet a proper waveform for the selected function is not obtained, this may be an indication of defective pattern logic circuitry. Refer to the TROUBLESHOOTING section (page 137) of this manual for further information.

Once power has been applied to the Model 2501 it is ready for operation. Pattern parameters and timing are entered by keypad. The operator may build a rate, each parameter at a time, or may choose standard proportion and format which will be computed automatically. The computerized sync generator allows rates to be stored, recalled for use, edited or deleted by keypad code entries. The function of each mode (BUILD, EDIT and RECALL) is described completely in PROGRAMMING AND USER CODES (page 75).

Software "lockout" is provided to prevent unauthorized editing without proper security password. The user cannot access the BUILD or EDIT modes unless this security password is entered. This safeguard prevents unauthorized entry, alteration, or deletion of information in storage.

The generator has been tested at the factory with several pre-programmed scan rates as itemized on RASTER SUMMARIES found in the RasterMaster Log. Any one of these scan rates can be deleted by following the procedure given in the Log. The Model 2501 enables storage of up to 69 separate rasters, access by two-digit code.

A basic set of test patterns is provided with selection made at the control panel. Each test pattern function is described in the OUTPUT SIGNALS section (page 37) of this manual.

The function of all controls is described fully in the FRONT PANEL CONTROLS (page 25) and INTERNAL CONTROLS (page 33) sections. The output signal should be routed to an appropriate display device for visual analysis of the pattern as described under CONNECTIONS (page 17).

REAR PANEL CONTROLS

TTL LEVEL PULSE POLARITY . . . . The TTL level pulse outputs (H Trigger, V Trigger, Blanking, Sync, H Sync, V Sync) are of selectable polarity, either positive or negative going pulses, by slide switch located next to the BNC output connectors. Each output has an individual switch so that polarity selection of one pulse is independent of another.

MASTER OSCILLATOR INTERNAL/ EXTERNAL . . . The selector slide switch allows choice of the the internal clock oscillator at 20 mHz or external clock, 2.0v. pk-pk square wave nominal. The external oscillator is intended to be near 20 mHz, to adjust counted vertical field rate.

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CIRCUIT CARD AND CONTROL LOCATIONS

CABINET LAYOUT

This instrument is packaged in a laboratory cabinet suitable for bench or rack mount use. It contains two card files plus the computerized sync generator card file. Text description is based upon orientation as outlined below.

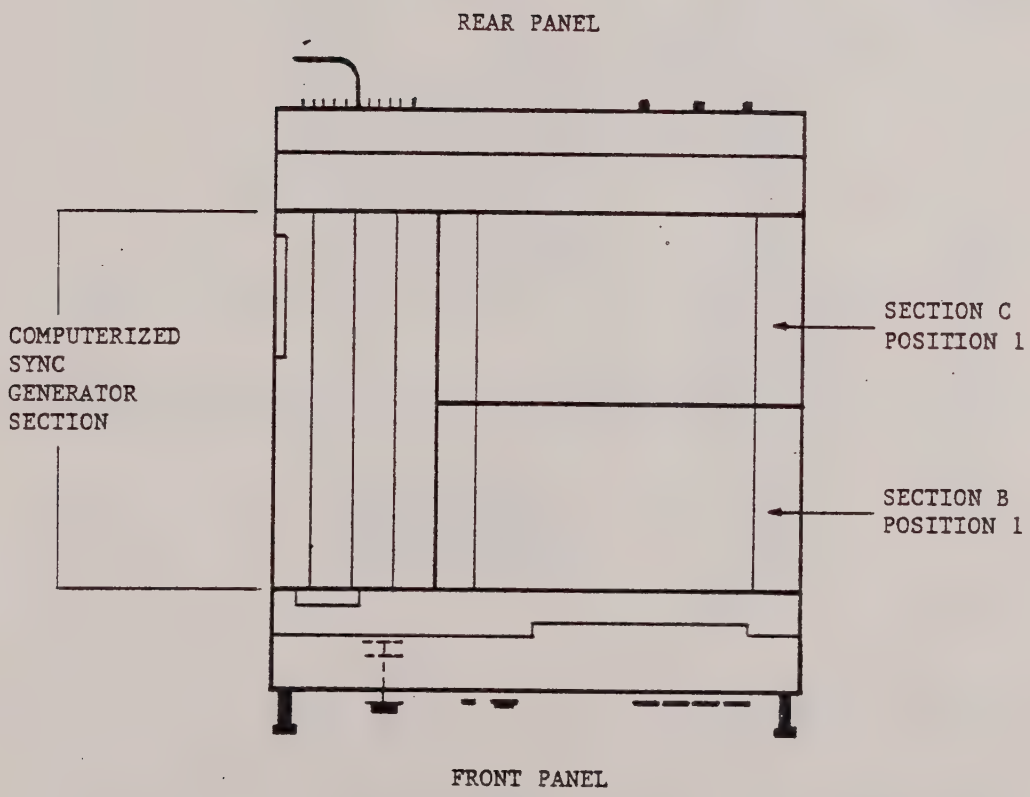

Figure 2 - Top View of Instrument

CIRCUIT CARD LOCATIONS

Circuit cards in the Model 2501 are located in positions listed below. Remove the generator top cover for access to internal controls. If the unit is rack mounted, it will be necessary to remove the instrument from the rack for cover removal and access to controls.

Insertion of cards into the improper slot may cause damage and, of course, the generator will be inoperative. Be sure to reinsert circuit cards into the correct location if they are removed, and establish that they are firmly seated into the connector. Cards are keyed so they cannot be inserted backwards; an attempt to force them in the wrong way will result in a broken connector.

SECTION B (Front)

Position	Dwg. No.	Name
1	- not used -	
2	- not used -	
3	4010-1	Video Control
4	4000-2	Gray Scale
5	4007-1	Gray Scale Select
6	4001-0	Video Clock
7	4002-0	Resolution Control
8	4003-2	Clocked Bar/Dot
9	4006-1	Pattern Logic
10	- not used -	
11	- not used -	
12	- not used -	
13	- not used -	
14	- not used -	
15	- not used -	
16*	2196-1	uP Interface
17**	2192-0	V Sync Generator
18**	2195-0	H Sync Generator
19	2190-0	CPU Sync Generator
20	2201-0	Power Interface
21	- not used -	

*uP Interface circuit board in Position 16 can be substituted for 4015 (uP Interface) also.

**H/V MPU Controlled Sync Generator (2221) may be used in place of the V Sync Generator (2192) and H Sync Generator (2195) circuit cards.

SECTION C (Rear)

Position	Dwg. No.	Name
1	- not used -	
2	2110-1	Power Regulator
3	2155-7	TTL Video - R
4	2155-8	TTL Video - G
5	2155-7	TTL Video - B
6	4008-1	Clocked Color Bar
7	4013-1	Resolution
8	4014-0	Character
9	4013-2	Resolution
10	- not used -	
11	2003-1	Pulse Output
12	2118-5	TTL Pulse Output
13	- not used -	
14	- not used -	
15	- not used -	
16*	2196-0	uP Interface
17**	2192-0	V Sync Generator
18**	2195-0	H Sync Generator
19	2190-0	CPU Sync Generator
20	2201-0	Power Interface
21	- not used -	

*uP Interface circuit board in Position 16 can be substituted for 4015 (uP Interface) also.

**H/V MPU Controlled Sync Generator (2221) may be used in place of the V Sync Generator (2192) and H Sync Generator (2195) circuit cards.

INTERNAL CONTROL LOCATIONS

Two sizes of circuit cards are used - large cards in the computerized sync generator which do not contain user controls, and pattern logic cards which do contain user controls, are smaller and in the format noted below. The circuit cards may vary in orientation for various instruments. Therefore, the description of control locations has been standardized as to location on the circuit card itself. Locations are keyed to the circuit card as viewed from component side, connectors down, as shown below:

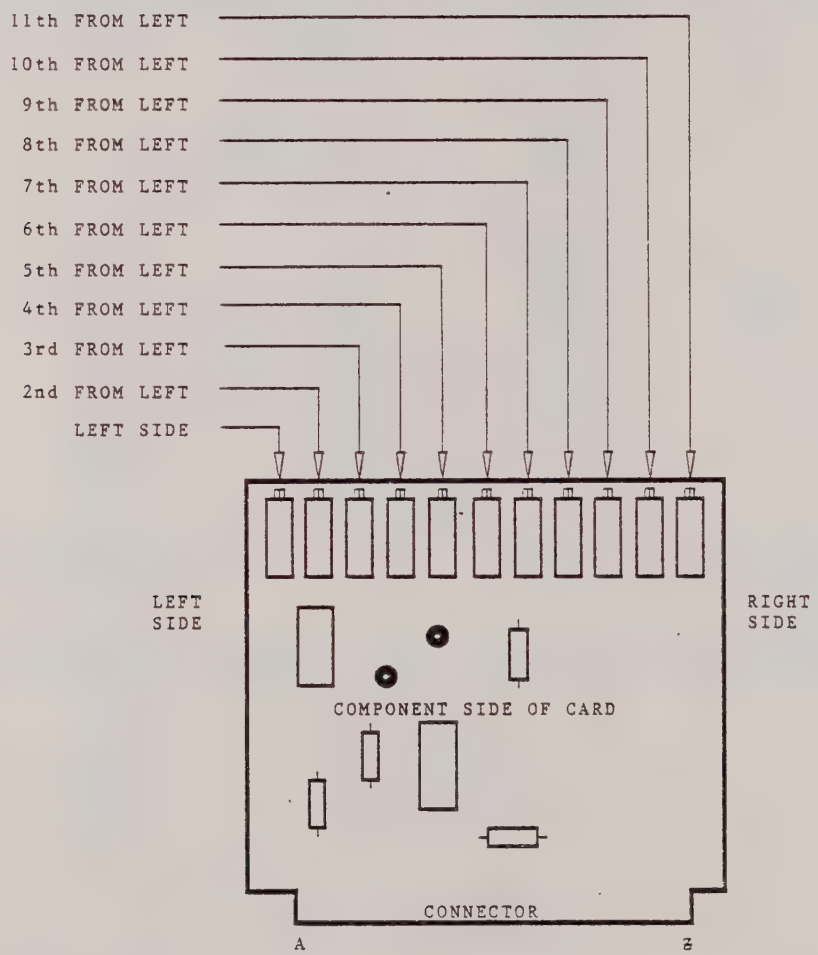

Figure 3 - Circuit Card Control Orientation

INTERNAL CONTROLS

Access to internal adjustments is by removal of the generator top cover; loose eight flathead screws and lift the cover for access to the interior. Circuit cards are located in positions listed on pages 30 and 31, CIRCUIT CARD LOCATIONS. Sections B and C are located as shown in Figure 2. Refer to Figure 3 for location of controls on the circuit cards.

Section B - (Front)

WHITE LEVEL . . . The control located at the right side on the VIDEO CONTROL (Position 3B) circuit card is used to establish maximum white video level.

BLACK LEVEL . . . The control located at the center of the VIDEO CONTROL (Position 3B) circuit card adjusts the d.c. level of the gray scale black level. A test point is also provided for oscilloscope observation of the signal output from the VIDEO CONTROL card while making black level adjustments.

GRAY SCALE STEPS . The GRAY SCALE (Position 4B) circuit card contains controls for adjustment of steps in the Gray Scale pattern (black and white levels at the extreme ends of the scale are fixed). These controls should be adjusted for the proper linear or other Gray Scale characteristic desired while observing the output signal waveform on an oscilloscope. Specific procedure for Gray Scale calibration is outlined in the PERFORMANCE VERIFICATION AND CALIBRATION section (page 93).

Gray Step 1 . . . 11th from left side
Gray Step 2 . . . 10th from left side
Gray Step 3 . . . 9th from left side
Gray Step 4 . . . 8th from left side
Gray Step 5 . . . 7th from left side
Gray Step 6 . . . 6th from left side
Gray Step 7 . . . 5th from left side
Gray Step 8 . . . 4th from left side

BURST APL . . . . The control located at third from left side on the GRAY SCALE (Position 4B) circuit card establishes a 50% gray level between each resolution burst in the Resolution pattern.

FLAT FIELD LEVEL . The control located at second from left side on the GRAY SCALE (Position 4B) circuit card is used to adjust flat field level, usually 50% of maximum white level.

100% WHITE FLAT FIELD LEVEL . Some applications require that the Flat Field be at 100% white level. Refer to OPTIONS IN OPERATION (page 21) for the circuit change required to accomplish this calibration.

WHITE/BLACK LEVEL . The control located at the left side on the GRAY SCALE (Position 4B) circuit card establishes level of the whiter-than-black portion of the Black Reference segment of the Video pattern.

Section C - (Rear)

SYNC LEVEL . . . . The control located at the left side on the TTL VIDEO circuit cards (Positions 3C, 4C, 5C) is used to vary the level of the sync that is inserted on the composite video signal. The output may be adjusted from zero to nearly 0.5v. The adjustment should be performed while observing the output signal on an oscilloscope. Each video channel is adjusted individually.

BLANKING LEVEL . . The control second position from left on TTL VIDEO circuit cards (Positions 3C, 4C and 5C) controls level of the blanking pedestal (setup) inserted into the composite video signal. Each video channel is adjusted individually.

COMP OFFSET . . . The control in the third position from left on the TTL VIDEO circuit cards (Positions 3C, 4C, 5C) is used to adjust the composite video blanking level (blacker-than-black) d.c. component. Usually blanking level is adjusted to ground (0v.) level.

VIDEO GAIN . . . The control fourth position from the left side on the TTL VIDEO circuit cards (Positions 3C and 5C only) is used to match the video level of the red and blue channels to the green channel video level.

BLACK LEVEL . . . The control located in the fifth position from the left side on the TTL VIDEO (Positions 3C, 4C and 5C) is used to adjust the Gray Scale black level to match the black level of digitally generated pattern elements. This control functions separately from the Black Level control on the VIDEO CONTROL (Position 3B) circuit card.

RESOLUTION BALANCE . . . The control at the left side on the RESOLUTION circuit card (Position 7C) is used to obtain the same width of alternate black and white resolution pattern elements. It is used in conjunction with the Resolution Rep Rate control in adjusting the resolution element line density.

RESOLUTION REP RATE . . . Controls to adjust precisely the repetition rate for the particular burst mode (1, 2, 3, 4 or 5), aspect ratio, and active line length in use. This adjustment should be made while observing bar width on a precisely calibrated oscilloscope, as described under PERFORMANCE VERIFICATION. Control locations on the RESOLUTION (Position 7C) circuit board are as follows:

Potentiometer E (right side) . . . . . Rep Rate 1
Potentiometer A (second from right) . . . Rep Rate 2
Potentiometer B (third from right) . . . Rep Rate 3
Potentiometer C (fourth from right) . . . Rep Rate 4
Potentiometer D (fifth from right) . . . Rep Rate 5

CHARACTER CLOCK . . . The control at the right side on the RESOLUTION circuit card in Position 9C adjusts the clock rate for Character development. This will vary the number of characters generated in each horizontal row across the display screen.

CHARACTER BALANCE . . . The control at the left side on the RESOLUTION circuit card in Position 9C is used to match the width of Character pattern elements to the space between these pattern elements.

PULSE AMPLITUDE . The control at the right side on the PULSE OUTPUT (Position 11C) circuit card adjusts simultaneously the amplitude of output pulses (H drive, V drive, blanking and sync) over a range of 3.5v. to 4.5v. peak-to-peak when properly terminated. Nominal setting is 4.0v. peak-to-peak.

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OUTPUT SIGNALS

Programmable Sync Generator Section

The synchronizing ("sync") generator produces pulses which are used to synchronize camera, display and other television devices in developing the t.v. raster. These pulses control the order in which the television picture will be produced. Four basic types of electrical pulse signals have become commonly used for such purposes, including H Drive, V Drive, Blanking and Sync, as described by EIA Standards RS-170, RS-330 and RS-343. All pulses are generated from a very stable master oscillator which is crystal controlled. Digital techniques are used to generate pulses at the horizontal and vertical rates of the scan rate to be used. These include:

H DRIVE is a pulse train in which a pulse starts at the end of every television scanning line. Its function is to mark the time interval between the end of one line and the start of another; the pulses may be used to control horizontal deflection "flyback" and signal processing. The pulse train is continuous, uninterrupted even during the vertical synchronizing interval. These pulses are useful for synchronizing an oscilloscope when inspecting the television waveform at horizontal line rate, provided in the Video format only.

V DRIVE is a pulse train in which a pulse starts at the end of each television field. Its function is to mark the time interval between the end of one television field and the next; these pulses may be used to control vertical deflection "flyback" and signal processing. These pulses are useful for synchronizing an oscilloscope when inspecting the television waveform at vertical field rate, provided in Video format only.

BLANKING is a mixture of horizontal and vertical information intended to control the "blackout" of the television system during deflection return between horizontal lines and vertical fields. These pulses are wider than drives or sync to insure that all transitions are made invisibly. This signal is provided in both TTL and Video formats.

SYNC is a complex combination of horizontal and vertical pulse information intended to control the decoding of a television signal by a display device, recorder or other type of video processing equipment. Usually it is mixed with the video information to produce a composite picture signal which is distributed for general use, and is provided in both TTL and Video formats.

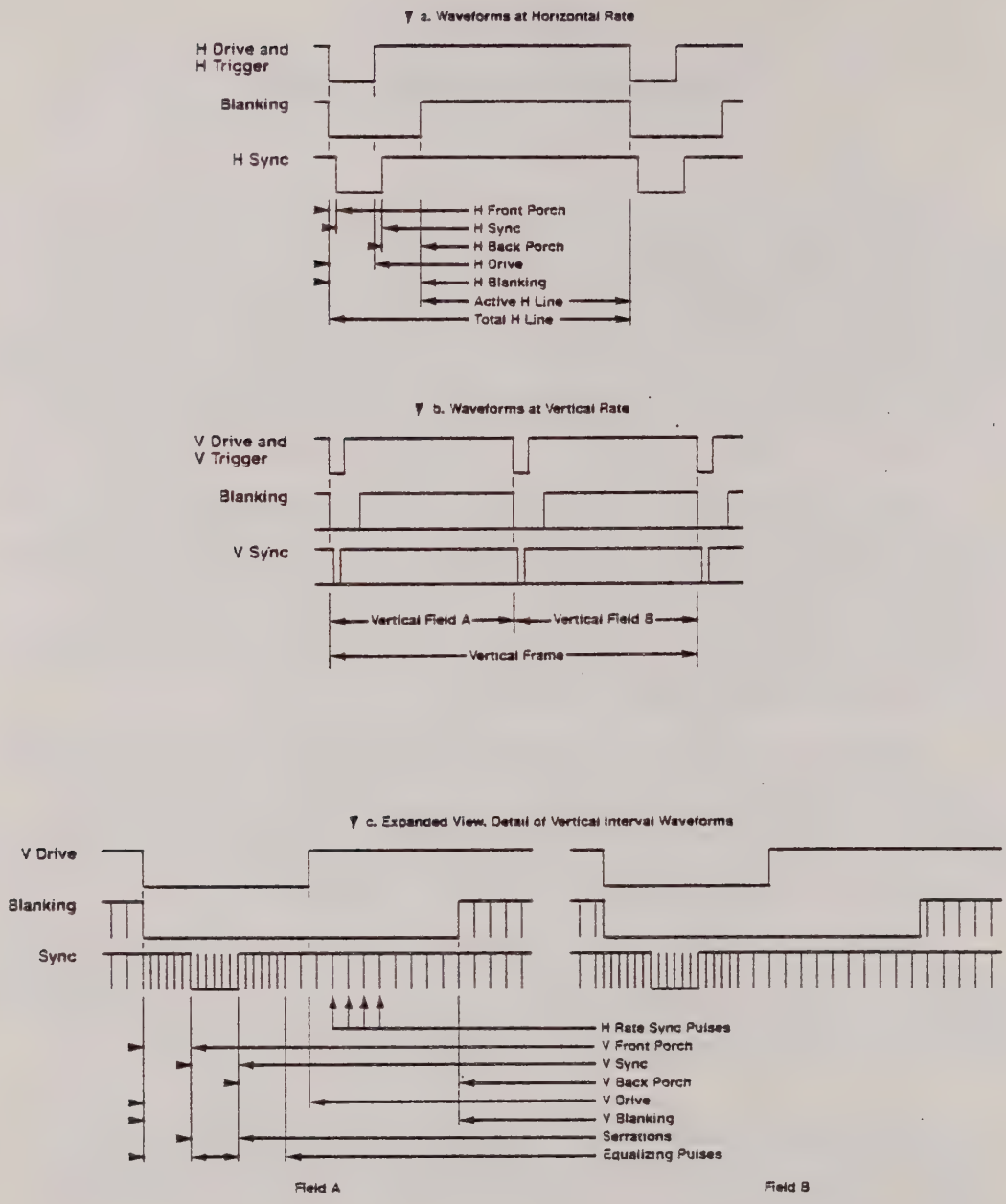


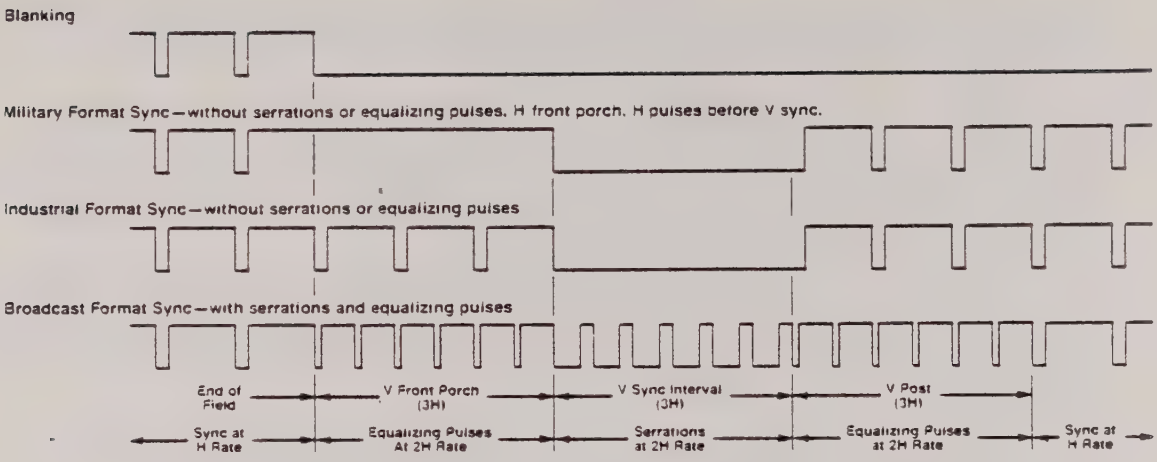
Figure 4 - Typical Sync Generator Output Waveforms

H SYNC is the horizontal sync pulse, as provided in the composite sync signal but is developed continuously even through the vertical interval. It is provided for the TTL format only.

V SYNC is a vertical rate pulse coincident with the vertical sync interval in the composite sync signal. The leading edge is fixed at three line intervals after the leading edge of V blanking. The V sync pulse width is three lines wide. Position and width are clocked, not adjustable, and is provided in the TTL format only.

H TRIGGER is a continuous, horizontal rate pulse train which is similar to H Drive, but both phase and width are adjustable, independent of H Drive. The leading edge may be adjusted to lead or lag the leading edge of H Drive. It is provided in TTL format only.

V TRIGGER is a vertical rate pulse similar to V Drive, but phase (position) and width may be selected independent of V Drive; position and timing is referred to the leading edge of V Drive.



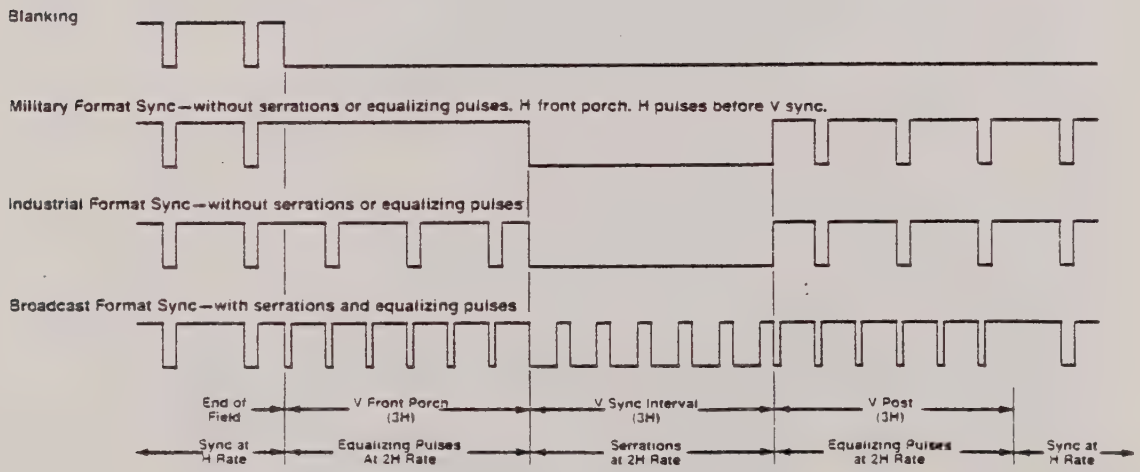
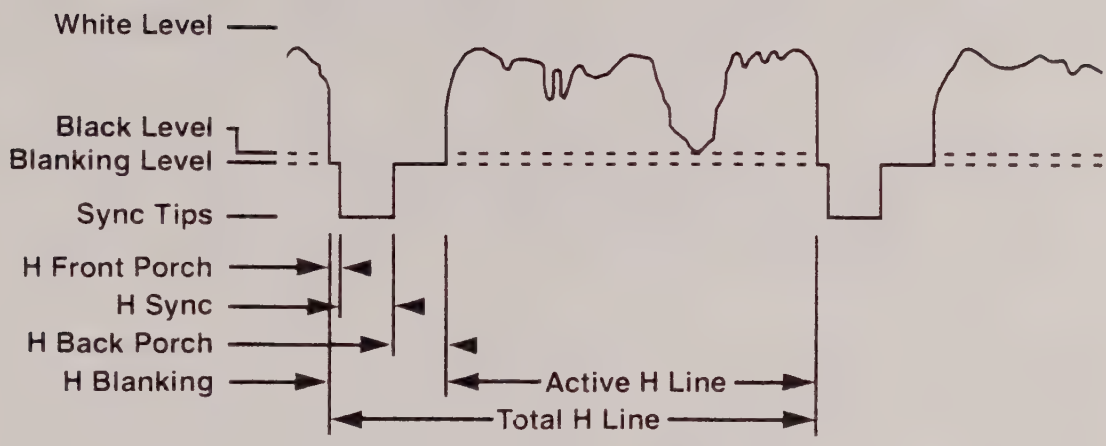
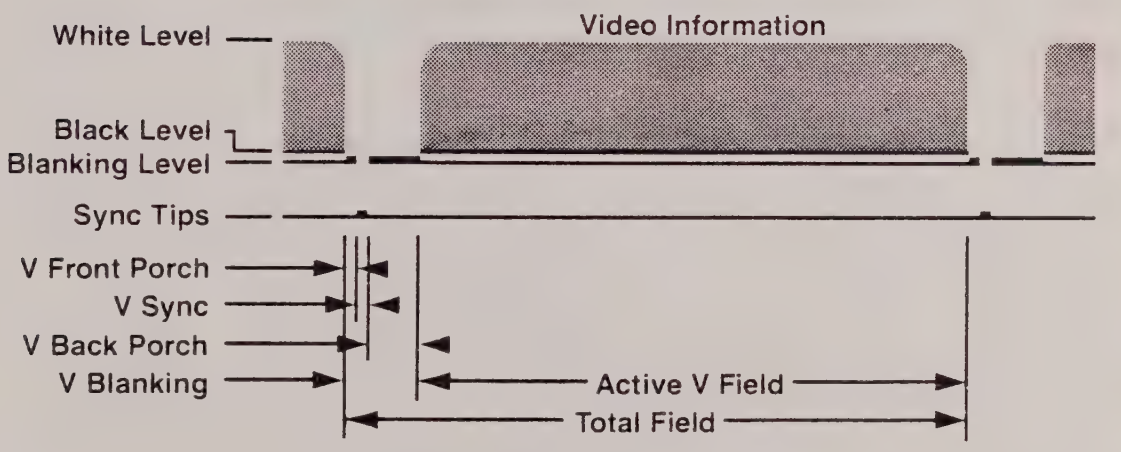


Figure 5 - Detail of Vertical Sync Interval,
2:1 Interlaced Raster



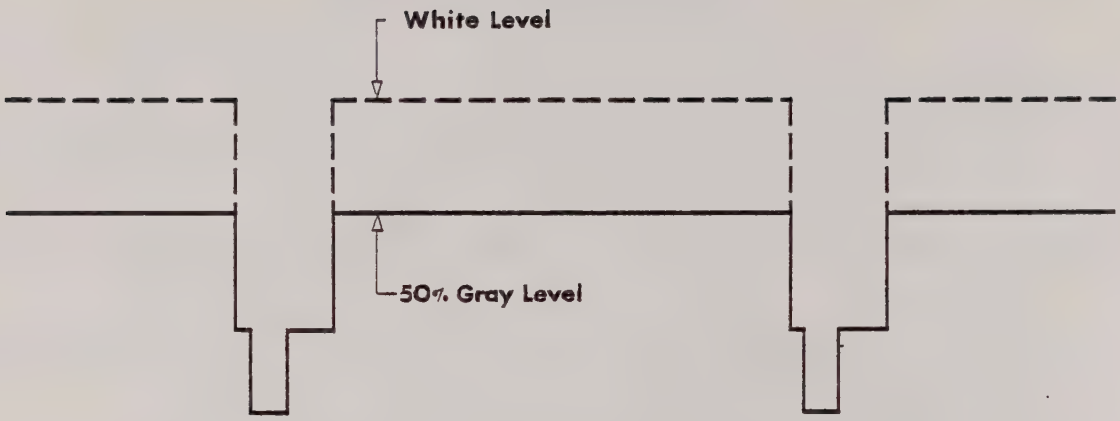
a. At Horizontal Scanning Line Rate



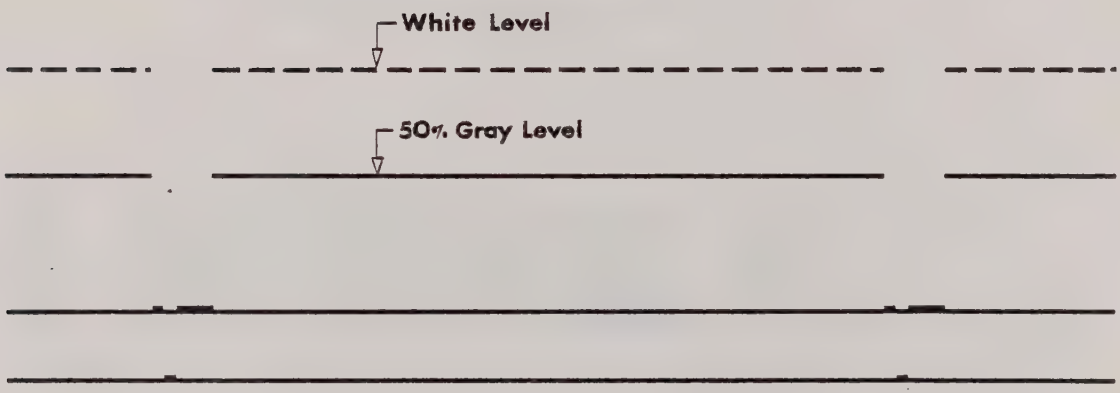
b. At Vertical Field Rate

Figure 6 - Typical Video Waveforms

The basic video signal is composed of video, blanking and sync as shown above to form the "composite video signal". Various significant parameters and common terminology applied to them (such as "front porch" and "back porch") are outlined above. In some instances, a "non-composite" video signal may be used which is the same as that shown above less the sync portion composed of only the video plus blanking.



a. Horizontal Rate



b. Vertical Rate

Figure 7 - Oscilloscope View of the FLAT FIELD Signal Waveform

FLAT FIELD

The Flat Field is an all-white, uniform signal of 100% duty cycle (APL). It represents a maximum load, and the uniform display permits evaluation of undesired brightness modulation which may be introduced into the display by the display device. Flat Field is adjusted normally to be 50% gray level to preserve 50% average picture level in the output pattern. Some applications require that Flat Field be at 100% white level. Refer to OPTIONS IN OPERATION (page 21) for the circuit change required to accomplish this calibration.

BARS and DOTS

The patterns of this category are all related, derived of common proportions. The Bars pattern (also referred to as "grating" or "crosshatch") is a grid pattern composed of horizontal and vertical lines. The Dots pattern provides a series of dots only at the location of the intersection of horizontal and vertical elements of the Bars pattern.

The Bars and Dots patterns have become universal in television size and linearity measurements. Yet care must be taken in application of these patterns, particularly in conjunction with use of the linearity charts. Extra caution is necessary when using the chart at scan rates other than 525/60, the rate for which traditional materials now in common use were designed.

The intended application of the Bars (crosshatch) and Dots patterns has great influence over the design of circuitry for producing that pattern. These patterns are intended for the measurement of deflection scan geometry, a term which includes linearity, size and other distortions which may occur due to component problems - such as skew, pincushion and barrel distortion. The method of measurement, almost universally accepted, is one that uses an electronically generated reference grid compared to a test chart. This technique is suitable for test of either a television camera or display device.

Modern television applications demand even greater accuracy in television displays. The response to this demand has been development of more precise test techniques to verify performance to the degree of precision desired.

The universally accepted method of measurement of scan linearity and geometry is an electrically generated reference grid compared to a test chart. This technique is suitable for test of either a television camera or display device. A camera is arranged to view the linearity chart. An electronically generated pattern, Bars or Dots, is superimposed on the camera output signal and the combination signal is displayed on a t.v. monitor for analysis. In a display device, the linearity chart usually is projected onto the display, although a direct overlay could be used; a Bars or Dots signal produces the electronic pattern on the display device for comparison. The electronically generated pattern, if accurately produced, will match the chart when scan is linear and without other distortions. A "perfect" scan will result in each electronically generated dot falling in the center of the chart circles.

This system for precision evaluation of scan geometry is standardized on the basis of the traditional 17 V Bars/14 H Bars pattern to a 4:3 aspect ratio, with H bar position variations as appropriate to accommodate the raster structure on each scan rate.

The chart-pattern comparison technique is quite powerful. It allows rapid analysis of size, centering and stability of these parameters. Abnormalities such as non-linearity, skew, barrel and pincushion are readily identified and may be evaluated in terms of numerical tolerance to as fine as ±0.25%. Several Technical Notes are available on this subject; contact the factory for further information.

Particular attention has been given to the position of V bars in the television raster. While various element placements have been used, the only pattern referred to in standards (RS-170 and IEEE-202) is the one shown in Figure 8.

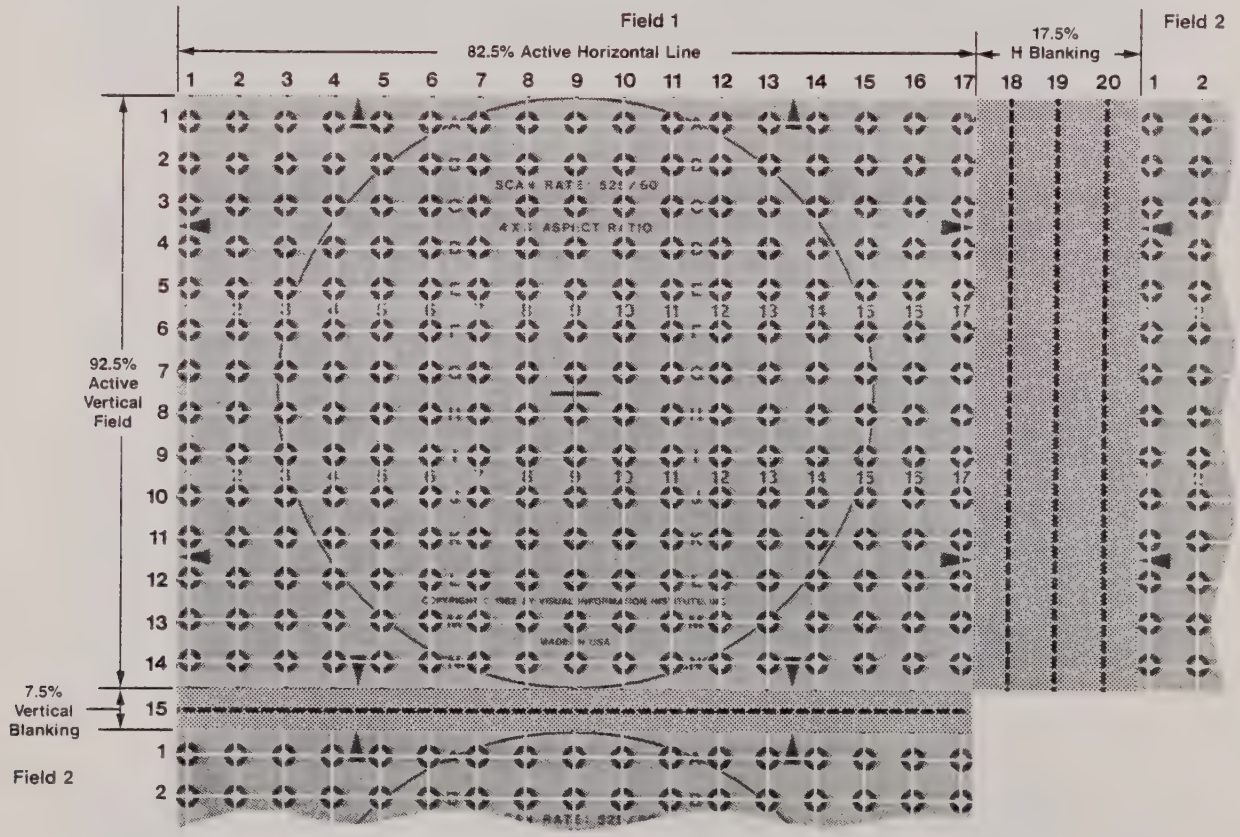


Figure 8 - Standard Bars Pattern
14 x 17 Format - 4:3 Aspect Ratio

Linearity charts contain 17 columns of circles in 14 rows. A typical chart is shown in Figure 9. Charts are customized for each scan rate; the placement of the 14 rows is dictated by the television raster structure as detailed in Table I. The 17 columns are positioned the same for all rates of the Vii standardized system.

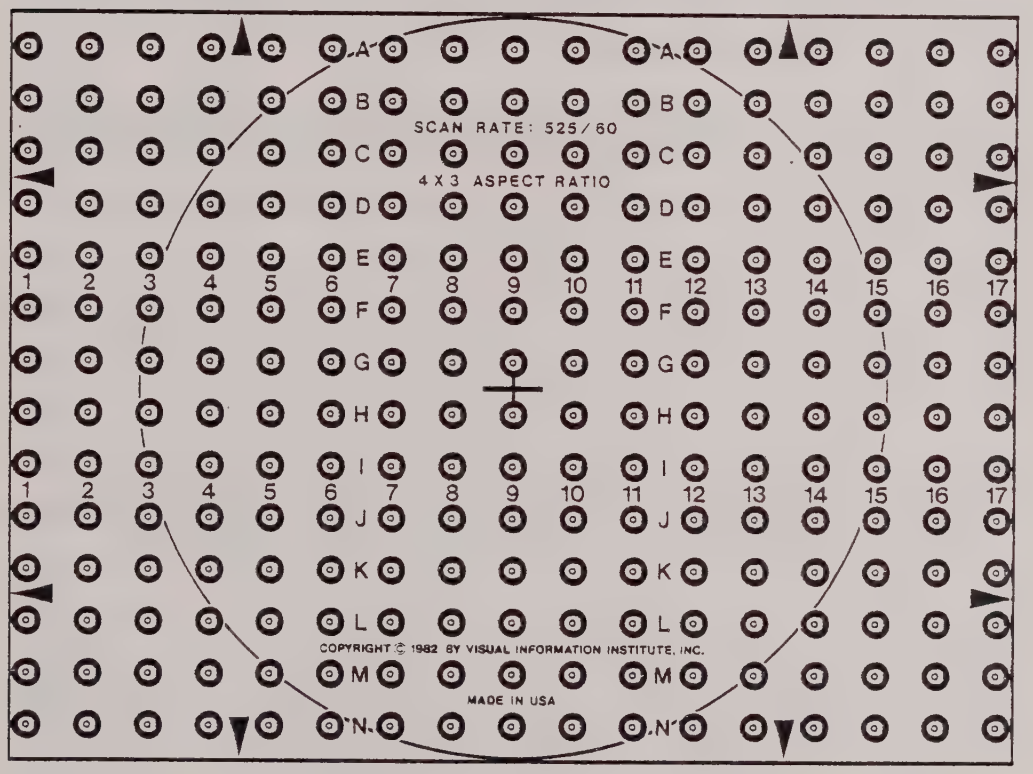


Figure 9 - Typical Television Linearity Chart

Circles in the chart are the same for all rates. They are drawn to represent a tolerance percentage of total active raster height. A circle whose radius is equal to 1% of display height represents a total of ±1% range. To be consistent with commonly accepted tolerances, the Vii chart circles are configured to represent ±2%, ±1%, ±1/2% and ±1/4% as shown in Figure 9.

Standard charts are available from Visual Information for the EIA standard scan rates of 525/60, 675/60, 729/60, 875/60, 945/60, 1023/60, 1029/60, 1225/60 and 625/50. Customized charts are available from Vii for other rates as well on a special order basis.

The user has a choice of two modes for pattern development of the Bars and Dots functions. Selection of either the STD or CUST mode is selected during programming. The STD mode automatically calculates position of vertical bar elements. The foundation for vertical bar element calculation is 20 elements per total line, including blanking. Since the horizontal blanking pulse is 17.5% of the total line, there are 17 visible V bars centered in the active area, yielding a 1.25% margin at each edge of the display. That is, the bars at left and right are set in from the edge by 1.25% of the total horizontal line time. Figure 10 shows vertical bar element proportion as produced by the H PATTERN (Parameter 20) STD mode. If standard proportion is not appropriate, spacing and position of vertical bar elements can be placed to suit any application using the CUST mode instead. The user may program position of the first vertical bar from the left side of the display and also spacing between vertical bars. Therefore, the placement and number of vertical bar elements is determined by program entry of Parameters 21 (V BAR POS) and 22 (V BAR SPC).

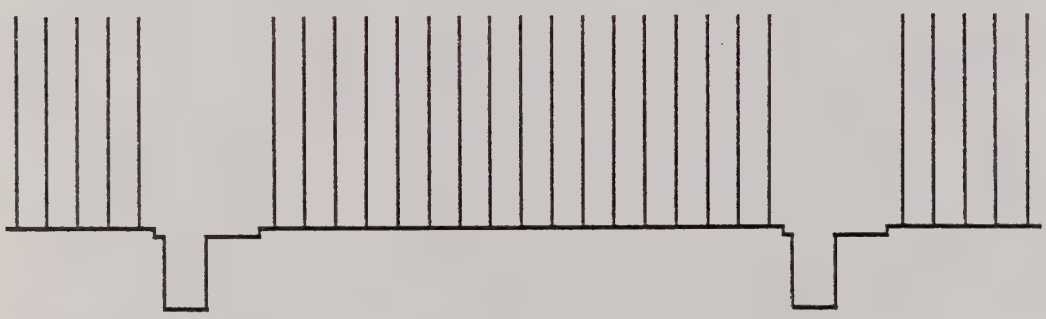


Figure 10 - Oscilloscope View of Vertical BAR Elements, Horizontal Rate

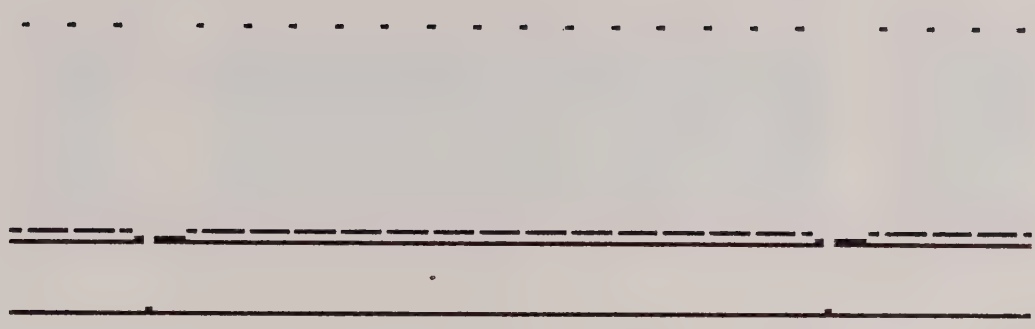


Figure 11 - Oscilloscope View of Horizontal BAR Elements, Vertical Rate

Calibration of horizontal bar elements is based upon, generally 15 equal elements developed in the total vertical field. One element would not be visible due to vertical blanking, leaving 14 visible H elements on the display. The user always must program position of the first horizontal bar element from the top of the raster and also spacing between adjacent H bars. The STD mode does not apply to horizontal bar elements. Position and spacing of horizontal bar elements are programmed, using Parameter 25 (H BAR POS) and Parameter 26 (H BAR SPC). H Bar locations have been standardized as shown on Table I for scan rates most commonly encountered. These locations are chosen to match linearity charts designed specifically for each scan rate. Contact the factory for H bar locations most appropriate for other rates not listed here.

It is necessary, in an accurately generated pattern, for the H bar element to occur for one complete scan line, positively locked so as to preclude drift or "run through" that will permit intensification of partial lines, etc. Otherwise an error of at least one scan line width can occur in the display of the pattern. Table I summarizes the scan lines which should be intensified to match the Linearity Chart as standardized by Vii. This is <u>not</u> compatible with the traditional EIA Linearity (Ball) Chart.

TABLE I

TV RASTER STRUCTURE TO MATCH LINEARITY CHARTS

H Bars - Scan Lines To Be Intensified

SCAN RATE	525/60	675/60	729/60	875/60	945/60	1023/60	1029/60	1225/60	U.S. 625/50	CCIR 625/50
BLANKING (lines)	20	26	28	33	36	39	39	41	20	25
TOP EDGE	0	0	0	0	0	0	0	0	0	0
H BAR NUMBER 1	11	13	12	14	17	15	17	17	10	8
2	28	35	36	43	48	49	51	58	31	29
3	45	57	60	72	79	83	85	99	52	50
4	62	79	84	101	110	117	119	140	73	71
5	79	101	108	130	141	151	153	181	94	92
6	96	123	132	159	172	185	187	222	115	113
7	113	145	156	188	203	219	221	263	136	134
8	130	167	180	217	234	253	255	304	157	155
9	147	189	204	246	265	287	289	345	178	176
10	164	211	228	275	296	321	323	386	199	197
11	181	233	252	304	327	355	357	427	220	218
12	198	255	276	333	358	389	391	468	241	239
13	215	277	300	362	389	423	425	509	262	260
14	232	299	324	391	420	457	459	550	283	281
BOTTOM EDGE	242.5	311.5	336.5	404.5	436.5	472.5	475.5	566.5	292.5	287.5
H BAR SPACING	17	22	24	29	31	34	34	41	21	21

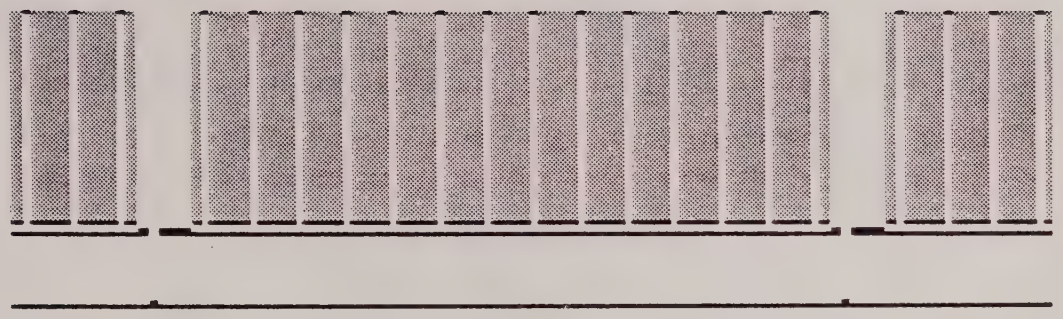


Figure 12 - Oscilloscope View of the BARS Signal Waveform, Vertical Rate

The Dots pattern provides a small dot of brightness at the points on the display at which the V bar and H bar elements intersect in the Bars pattern, and therefore are located by Bars pattern calibration.

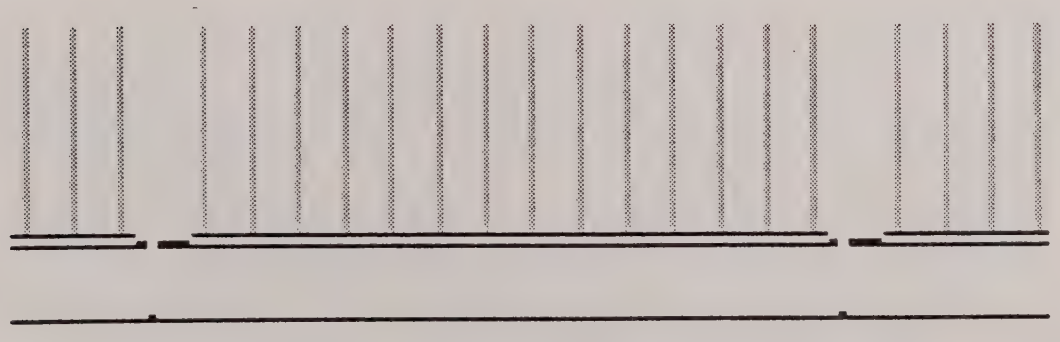
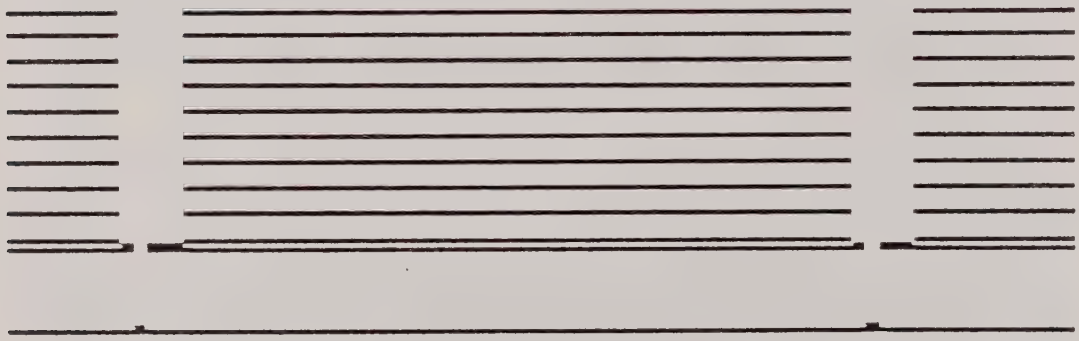


Figure 13 - Oscilloscope View of the DOTS Signal Waveform, Vertical Rate

a. Horizontal Rate



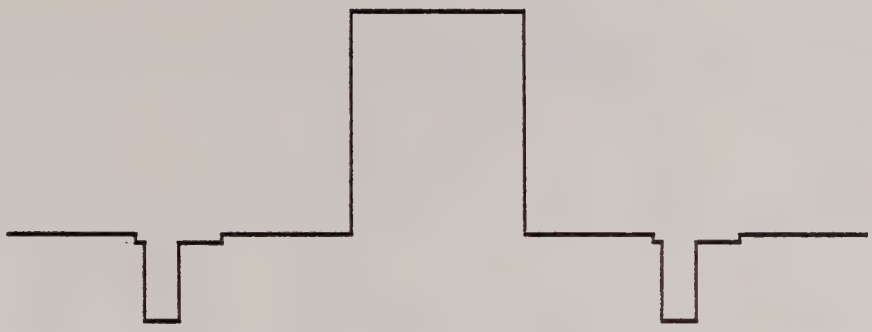
b. Vertical Rate

Figure 14 - Oscilloscope View of the GRAY SCALE Signal Waveform

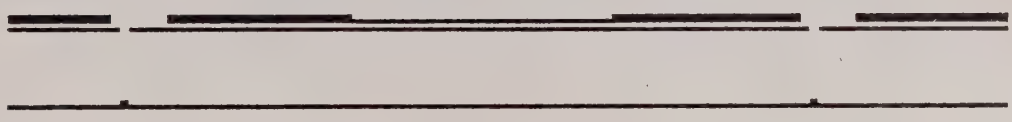
GRAY SCALE

The Gray Scale signal is composed of ten levels of brightness, including black and white. Therefore the traditional "ten step" scale actually is composed of nine risers, and eight shades of gray between the extremes. Gray Scale position is automatically determined by the computer and is not adjustable. Existing standards and common practice call for a linear Gray Scale test signal (one with all steps of equal amplitude).

The signal as described above provides a nominal 50% APL (Average Picture Level), representative of "typical" television scenes.



a. Horizontal Rate



b. Vertical Rate

Figure 15 - Oscilloscope View of the WINDOW Signal Waveform

V STRIPE and WINDOW

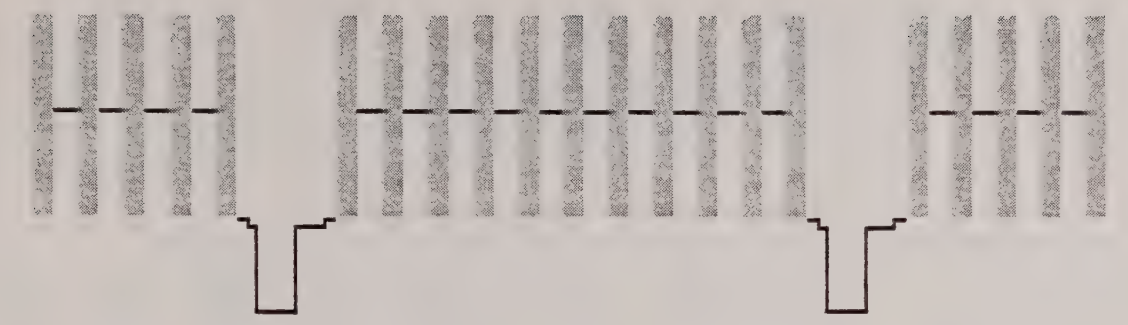
The Window is a white rectangle surrounded by a uniform black background over the remainder of the raster. This pattern provides a thorough evaluation of low frequency response, as evidenced by tilt in the vertical rate waveform. The sharp transition from black to white and white to black at the edges of the Window in the horizontal dimension provides a convenient tool for analysis of transient response also.

V Stripe is a strip the entire height of the display whose width is the same as the Window rectangle. This pattern usually provides 50% duty cycle (APL), thus preventing the development of distortion which may be present during the lower APL of the Window signal. Therefore, the transient response and mid-frequency response can be evaluated without distortion due to low frequency defects.

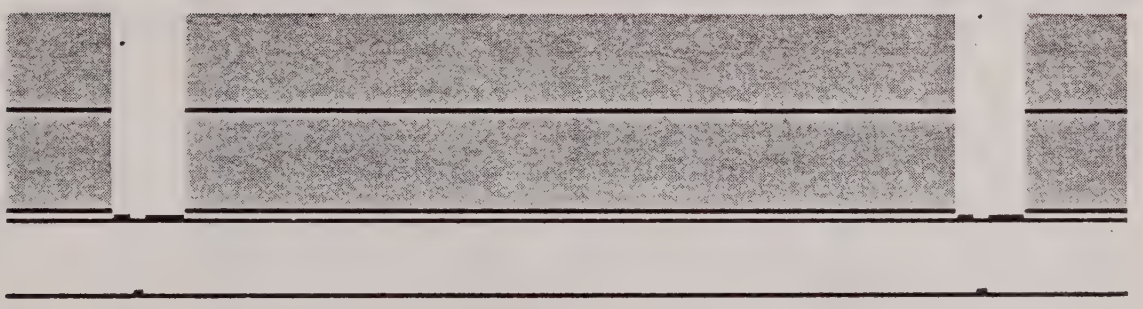
The waveform of the V Stripe pattern is the same as shown in Figure 15a, except that the center area will be brighter than in the Window waveform since the elements are developed in every line of the active raster rather than just a few.

The user has a choice of two modes for pattern development of the V Stripe function; either the STD or CUST mode is selected during programming. Standard V Stripe proportion of the white area is 0.50h (50% of the active portion of the horizontal line). This parameter is automatically calculated with the STD mode for H PATTERN (Parameter 20). Figure 15a shows the horizontal window as programmed by the H PATTERN STD mode. If standard proportion is not appropriate, parameters can be developed to suit any application using the CUST mode instead. The user may program width to suit any application by program entry of Parameter 23 (H WIN START) and Parameter 24 (H WIN STOP).

Horizontal width of the Window is always the same as that of the V Stripe. The user always must program height of the Window rectangle, usually to provide a window height of 0.50v (50% of the vertical portion of the vertical field) at the V WIN START (Parameter 27) and V WIN STOP (Parameter 28) prompts. The STD mode does not apply when programming vertical window parameters as is the case with programming horizontal window placement.



a. Horizontal Rate



b. Vertical

Figure 16 - Oscilloscope View of the RESOLUTION Signal Waveform, Bursts Mode at Medium APL

RESOLUTION

By common practice and standards definition, television resolution is the ability of the system to produce an alternate black and white line structure. Each line, black or white, is counted (as opposed to the common "line-pair" terminology of photography). Specifications of t.v. lines are related to the vertical dimension of the aspect ratio (ratio of horizontal size to vertical size).

The test pattern for resolution is generated electronically as a square wave, providing alternate black and white images in the display. Generally, the bursts are calibrated in 100 line increments, as shown in Figure 16. Alternate calibration provides bursts of resolution at any one selected resolution rate, or a continuous presentation of the desired rate over the entire active raster, as shown in Figure 17. Signal timing required to develop the desired "t.v. lines" at various scan rates is shown in Table II.

TABLE II

CCTV RESOLUTION TIMING
4 x 3 Aspect Ratio

A. EIA Format Standard Scan Rates

RESOLUTION - T.V. LINES		100	200	300	400	500	600	700	800	900	1000
ACTUAL, H LINE		133	266	399	533	666	799	933	1066	1199	1333
SCAN RATE (lines)	ACTIVE H LINE (usec)	TIME PER CYCLE (LINE PAIR) (nsec)									
525/60	52.5	789	395	263	197	158	131	113	98	88	79
675/60	42.4	638	319	213	159	127	106	91	80	71	64
729/60	38.7	582	291	194	145	116	97	83	73	65	58
875/60	31.1	468	234	156	117	93	78	67	58	52	47
945/60	28.3	426	213	142	106	85	71	61	53	47	42
1023/60	25.6	385	192	128	96	77	64	55	48	43	38
1029/60	25.4	382	191	127	95	76	64	54	48	42	38
1225/60	20.2	304	152	101	76	61	51	43	38	34	30
625/50	52.8	794	397	265	198	159	132	113	99	88	79

B. Vii Proportional Format Standard Scan Rates

RESOLUTION - T.V. LINES		100	200	300	400	500	600	700	800	900	1000
ACTUAL, H LINE		133	266	399	533	666	799	933	1066	1199	1333
SCAN RATE (lines)	ACTIVE H LINE (usec)	TIME PER CYCLE (LINE PAIR) (nsec)									
525/60	52.4	788	394	263	197	157	131	112	98	87	79
675/60	40.8	614	307	205	153	123	102	87	77	68	61
729/60	37.7	567	283	189	141	113	94	81	71	63	57
875/60	31.4	472	236	157	118	94	79	67	59	52	47
945/60	29.1	438	219	146	109	87	73	62	55	49	44
1023/60	26.9	405	202	135	101	81	67	58	50	45	40
1029/60	26.7	402	201	134	100	80	67	57	50	45	40
1225/60	22.4	337	168	112	84	67	56	48	42	37	34
625/50	52.8	794	397	265	198	159	132	113	99	88	79

In the 4:3 aspect ratio, in which the horizontal dimension is 1-1/3 times the height, there are actually 1-1/3 times the lines displayed as stated by the specifications. For example, a specified 100 t.v. lines will actually produce 133 elements across the horizontal scanning line, alternately black and white. This signal is used primarily to test horizontal resolving capacity of the system.

a. Horizontal Resolution . . Television horizontal resolution is specified as the number of lines, alternate black and white, which can be resolved in the length of scanning line equal to the height of the raster.

Tests of resolution usually are conducted at a 50% APL, as produced by a continuous, alternate black-and-white resolution line pattern. When a series of bursts is generated, the space between bursts is generally provided at a 50% gray level to preserve the medium APL, as shown in Figure 17.

b. Vertical Resolution . . Resolution in the vertical plane is dependent upon the number of scanning lines in the vertical raster dimension. An exacting description is complicated by the fact that "horizontal" scanning lines are not truly horizontal but are pitched slightly by the vertical deflection which occurs during a line period. The error is slight, varying with the number of scanning lines produced in the t.v. field. In most circumstances, the error is so slight that an analysis of the television scanning line will truly indicate vertical resolution.

This generator provides a reference signal for resolution - a relatively low frequency 50% duty cycle square wave which represents 100% contrast. Therefore, one has a frame of reference to evaluate contrast reduction which might occur with the higher frequency bursts.

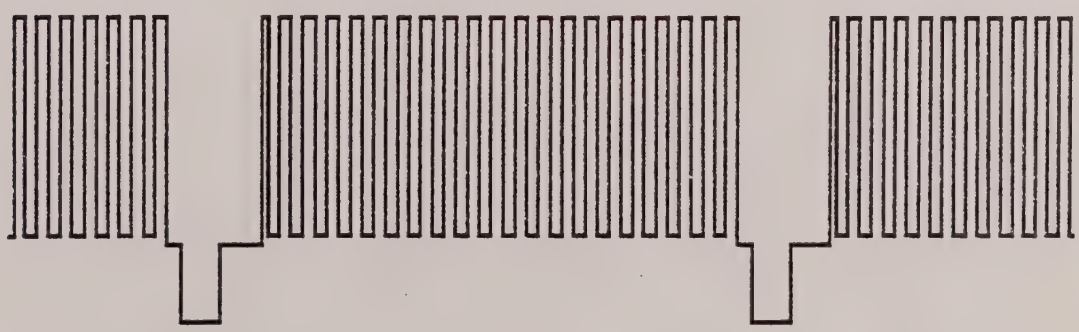
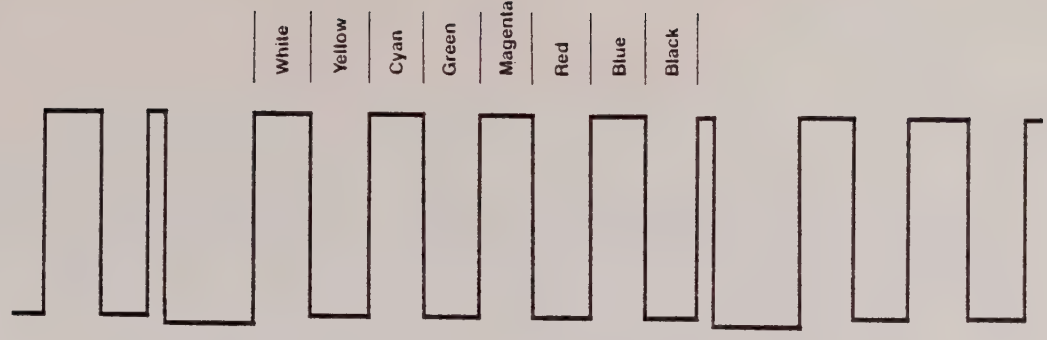


Figure 17 - Oscilloscope View of a Typical
RESOLUTION Reference Signal

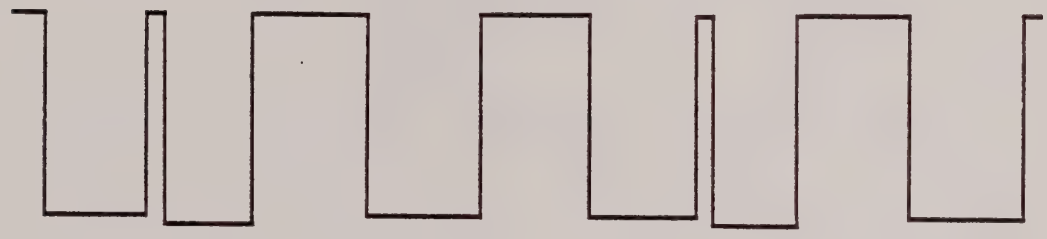
An inspection of Flat Field signal for sharp presentation of scanning line structure will provide an adequate prediction of vertical resolving capacity. Consideration must be given to the number of lines not displayed due to the vertical blanking interval. It is presumed that vertical resolution capacity is equal to the number of ACTIVE scan lines per frame. However, part of the raster may be obscured by overscan, and not useable.

For demanding tests, the scanning line number can be modified by the Kell factor as a further prediction of resolution in the actual vertical plane. This figure has been established at 0.7 for the 525-line rate, but has not been determined for other scan rates. Generally it is believed to be higher for increased numbers of scanning lines. Since the figure is derived from subjective tests, its use is not recommended.

Vertical resolution tests can be extended to provide a complete analysis of possible limiting resolution by use of scanning line profile analysis.



a. BLUE Channel Output Signal (Non-composite)



b. RED Channel Output Signal (Non-composite)

c. GREEN Channel Output Signal (Composite)

Figure 18 - Oscilloscope View of the COLOR BARS Signal Waveform

COLOR BARS

The Color Bars pattern generated by the video waveform is formed by gating the three output channels, as shown above, in proper sequence to develop colors as illustrated in Figure 18. All three channels should be at the same amplitude for standard measurement conditions. The white segment normally remains at 100% level. This pattern does include a narrow black margin at the left side and a narrow white margin at the right side to allow for possible overscan of the display device without obscuring Color Bar segments.

A common system configuration is to have a composite video signal on the green channel, and a non-composite signal on the red and blue channels by adjustment of sync level to zero on these channels, as shown above. The user can obtain a Non-composite or Video Only signal on all three output channels by circuit card control.

VIDEO

The Video test pattern is a video composite of various patterns recognized essential in the performance evaluation of various devices, including displays, recorders, scan connectors, transmitting links and various other video processing devices. They include Resolution, a series of closely spaced, alternate black and white bars representing fine detail; "Blacker-than-Black" Reference, sometimes referred to as the "pluge signal", a blanking level reference used as a visual reference to properly set the proper black level to a television display; Gray Scale, a sequence of steps from black level to white level at various video "shades of gray". Waveforms of this signal are shown in detail in Figure 19.

Resolution

By common practice and standards definition, television resolution is the ability of the system to produce an alternate black and white line structure. Each line, black or white, is counted (as opposed to the common "line-pair" terminology of photography). Specifications of t.v. lines are related to the vertical dimension of the raster to provide uniformity in specifications regardless of the aspect ratio (ratio of horizontal size to vertical size).

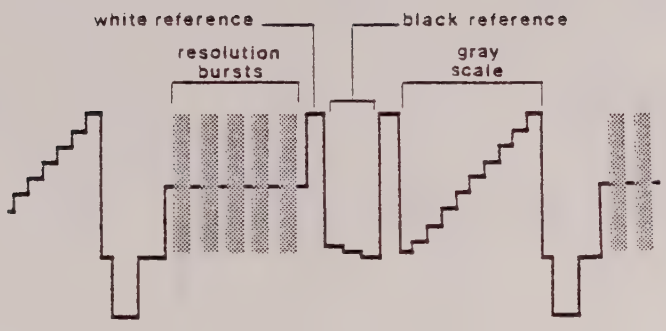
This signal produces a pattern on the display which tests the horizontal resolution capability of the device under test. Television horizontal resolution is specified as the number of lines, alternately black and white, which can be resolved in the length of scanning line equal to the height of the raster.

In the 4:3 aspect ratio, in which the horizontal dimension is 1-1/3 times the height, there are actually 1-1/3 times the lines displayed as stated by the specifications. For example, a specified 100 t.v. lines will actually produce 133 elements across the horizontal scanning line, alternately black and white.

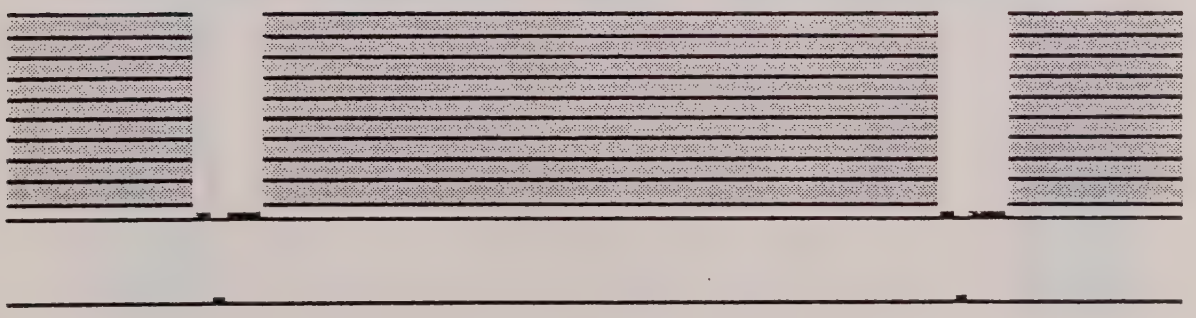
Tests of resolution usually are conducted at a 50% Average Picture Level (duty cycle). When a series of bursts is generated, the space between each burst is generally adjusted to a 50% gray level to preserve the APL to that level encountered in the "typical" television scene.

The test signal for resolution is generated electronically as a square wave, providing alternate black and white images in the display. Generally, the bursts are calibrated in increments of ascending order. Each of the five bursts can be adjusted independently providing repetition rates as desired within the capabilities of the instrument.

The resolution content is determined by selection of component values on the RESOLUTION circuit card (S-4013) in Position 7C. See PERFORMANCE VERIFICATION (page 93) for further details.



a. Typical VIDEO Test Pattern at Horizontal Rate, Delayed Oscilloscope Sweep to Show Individual Television Lines



b. Typical VIDEO Test Pattern at Vertical Rate

Figure 19 - Oscilloscope Views of the VIDEO Test Pattern Signal Waveform

Black Reference

The Black Reference signal is composed of three vertical strips of video at or near black level with maximum contrast, white reference levels at the left and right sides of the display. The center strip is at black level. The strip left of center is at gray level slightly above black level. The strip right of center is at blanking level, referred to as "blacker-than-black". This pattern is used to precisely set the black level and contrast of a display device. When properly adjusted the display will produce maximum specified white level at the left and right reference areas, the left and center strips will merge appearing as one wide black strip, and the right strip will appear separate at a gray level slightly above black. This pattern is utilized only at maximum level; the gray level strip will be reduced in amplitude at lower video levels.

Gray Scale

The Gray Scale signal is composed of ten levels of brightness including black and white. Therefore, the traditional "ten step" scale actually is composed of nine risers, and eight shades of gray between the extremes. The signal also contains a white flag before the ascending scale to provide a 100% contrast reference at the start of the Gray Scale segment.

Existing standards and common practice call for a linear Gray Scale test signal (one with all steps of equal amplitude). This provides a nominal 50% APL (Average Picture Level) representative of "typical" television scenes.

Each step is individually adjustable, so that the exact characteristic desired - linear, logarithmic, etc. - can be obtained.

COMBINATION

The Combination test pattern consists of the Video pattern plus Color Bars in one raster simultaneously. A strip of video appears through the color bars segment of the Combination pattern at approximately 20% raster height. The height of the video portion can be adjusted per user's discretion by programming changes.

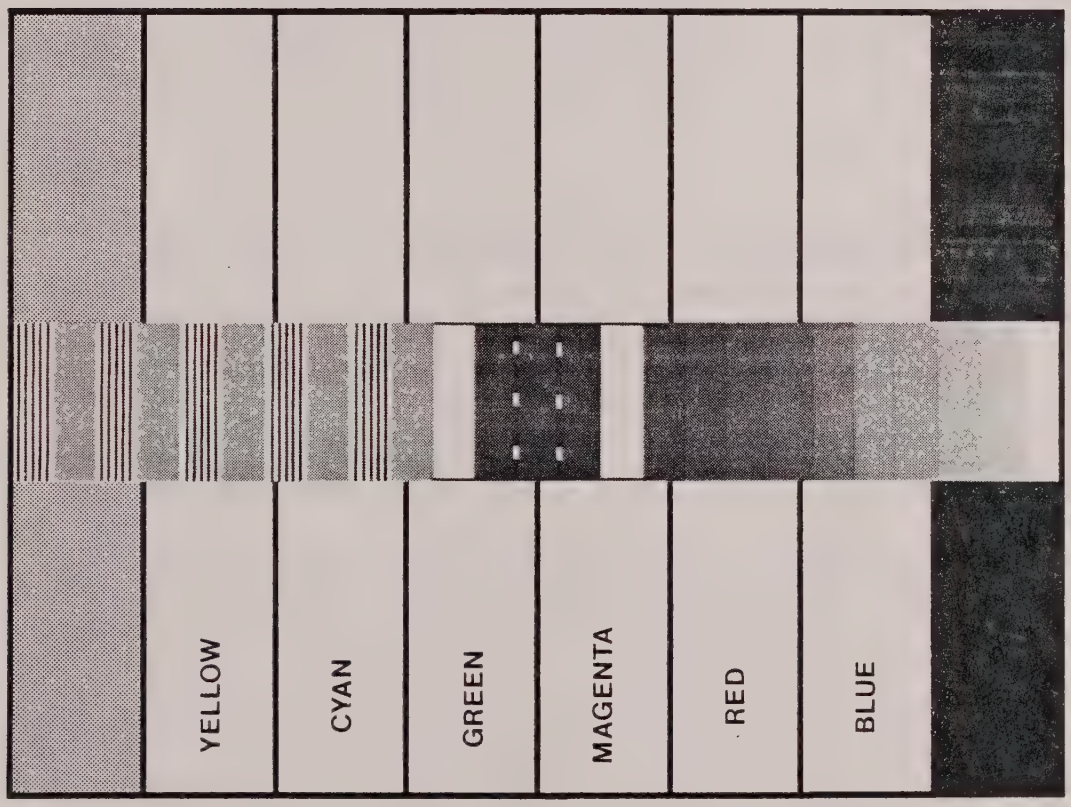


Figure 20 - Typical COMBINATION Test Pattern

CHARACTER

The choice of character, format and spacing is somewhat arbitrary. There is no standard or prevailing common practice to serve as guidance in determining what this function should provide. In lack of better precedent, Vii has chosen the following character as a "standard" product:

Character	[x]
Format	Five pixels wide by seven pixels (t.v. lines) high.
Spacing	Five pixels separation horizontally, three pixels (t.v. lines) separation vertically.
Duty Cycle	50% or 100% as selected by circuit card jumper.
Maximum Clock Rate . .	20 mHz

Often the "number of characters per row" is of interest. Yet this is a somewhat arbitrary specification dependent upon the clock rate, the horizontal active line time, the character format and spacing. The important parameter is the maximum clock rate that is possible. For instance, a clock rate of 20 mHz dictates a minimum dot time of 20 nsec. (50% duty cycle) or 50 nsec. per pixel at 100% duty cycle. Therefore, a character which is five pixels wide occupies 250 nsec. If characters are spaced apart five pixels, another 250 nsec. is consumed. Therefore, one character can be presented every 500 nsec. In a typical "standard" television system of the 525/60 scan rate, the active line time is 52.5 usec. In this case, it is possible to develop 105 characters per row. Higher performance scan rates have a shorter active line time, so the number of characters per row is dependent upon the parameters of the particular scan rate in use. For instance, with the 1023/60 scan rate, which has a 25.6 usec. active horizontal line time, 51 characters per row can be developed with the 20 mHz clock rate.

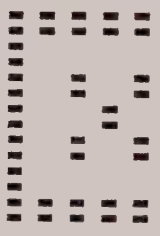
The number of rows is an often quoted specification. This is dependent upon the character format and the number of active horizontal scan lines in the vertical dimension of the raster. For example, the "standard" 525/60 scan rate is interlaced, and develops 262.5 scan lines per field. Vertical blanking consumes 20 t.v. lines, yielding 242.5 active lines per field. In a character format of 5 x 7 pixels, a character consumes seven t.v. lines. Some spacing between rows is necessary for clarity, possibly three active lines. Therefore, a character row may consume ten active lines in the 525/60 scan rate system. Of course, higher performance systems can develop more

rows of characters since more scanning lines are present, the 1023/60 rate, interlaced 2:1, has 472.5 active lines per field allowing generation of 47 rows of characters. In summary, a system using a 20 mHz clock rate can display:

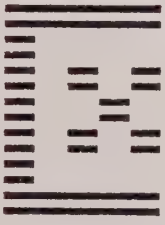
1. 105 characters per row and 24 rows in a system using the 525/60 scan rate;

2. 51 characters per row and 47 rows in a system using the 1023/60 scan rate.

The effect of interlace on the character must also be considered. Interlace produces two television fields per frame, in effect "doubling up" the information presented in the vertical display dimension. This causes horizontal lines to appear to be doubled in width, making a thicker, heavier looking character. Use of non-interlace is becoming more prevalent to allow more rows of lighter characters.



a. 50% Duty Cycle



b. 100% Duty Cycle

Figure 21 - T.V. Monitor Display of the CHARACTER Function, 2:1 Interlace

While the 2:1 interlaced raster will always produce two adjacent scan lines intensified, as shown in Figure 21, the use of a 1:1 interlaced (or non-interlaced) raster will produce the character with finer detail as shown in Figure 22.

a. 50% Duty Cycle

b. 100% Duty Cycle

Figure 22 - T.V. Monitor Display of the CHARACTER Function, 1:1 Interlace

Of course, the selection of a character shape and the 10 x 10 pixel format (5 x 7 active) is also arbitrary. For test purposes, it was felt desirable to have small characters spaced well apart for clarity. The block "C" with superimposed "x" was chosen because it contains straight lines in both horizontal and vertical planes, plus the "x" includes diagonal information.

Some firms have developed other formats of characters for testing. Vii can provide about any character desired for your particular application, as a prom is used for this function. Please contact the factory for further information. One thing to remember, the test instrument is not intended to be a full capability character generator. It is designed to provide the means for display performance evaluation and, therefore, produces only one style of character for this purpose.

All characters are identical, a block form upper case "C" with a lower case "x" superimposed. The character can be developed in either 50% or 100% duty cycle format, as shown on the previous page.

Waveform analysis is of little value in interpreting quality of the Character function. It is more convenient to view the Character display on a television monitor to assess quality.

DESCRIPTION OF A SCAN RATE

This instrument has been designed for operation at various scan, field and frame rates. This includes all rates specified by American EIA Standards RS-170, RS-330 and RS-343 which specify field and frame rates at 60 Hz and 30 Hz respectively, plus European rates which employ a 50 Hz field rate and 25 Hz frame rate, and other non-standard rates having from 10 usec. to 100 usec. total horizontal line times. Operation in a 2:1 interlaced or non-interlaced condition (1:1) is possible by proper selection of scan rate as described below. Commonly used pulse proportions are shown on Table III, page 72. Contact the factory if pulse width values for non-standard scan rates are desired.

A scan rate is determined by the number of scan lines per field and the desired field repetition rate. The master counter determines the rate at which horizontal lines are developed and that, in turn, determines what the frequency or repetition rate of the television field will be. By definition of 2:1 interlace, two fields constitute a frame; a frame is defined as one complete presentation of raster information. Therefore, the designation of 525/60/30 indicates that:

a. There will be 525 horizontal scan lines per frame.

b. The field rate shall be 60 Hz.

c. The frame rate shall be 30 Hz.

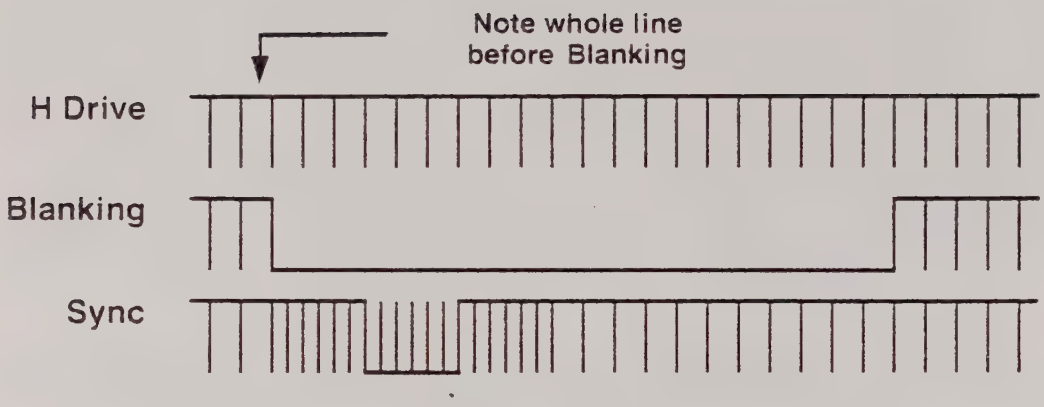
d. The ratio of field repetition rate to frame repetition rate determines the interlace ratio will be 2:1, which indicates that there will be two fields per frame, each field containing one-half of the total scanning lines - in this case 262.5.

Television systems operate at many different scan rates. Complete specification of a rate requires information to completely define the following.

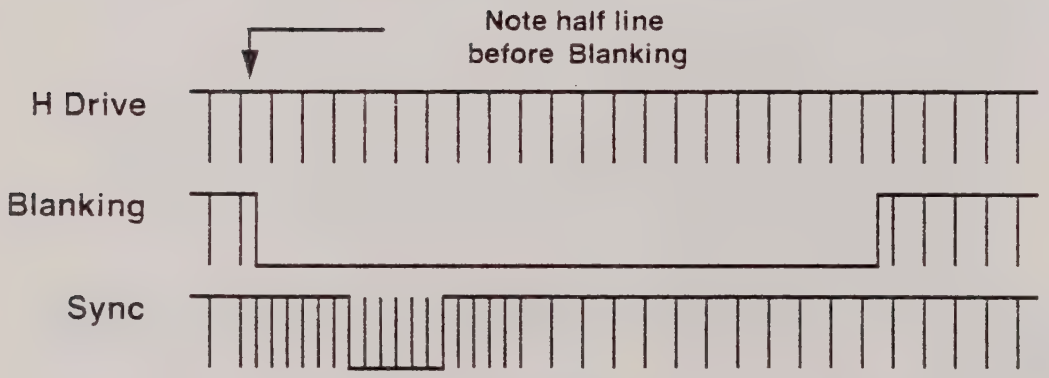
- Horizontal scanning line repetition rate (usually in kiloHertz, kHz).

- Number of scanning lines to be developed in two television fields.

- The number of television fields which make up a complete frame.



a. Start of "Even" Television Field



b. Start of "Odd" Television Field

Figure 23 - Detail of 2:1 Interlace

- The width of pulses present within the various synchronizing waveforms:

H Drive	H Blanking
V Drive	V Blanking
H Sync	H Front Porch
2H Serrations	2H Equalizing
H Trigger Position	H Trigger Width

Most television systems are "interlaced" to avoid a visible flicker in the display, usually at 2:1 ratio. Thus 2:1 interlace ratio means that two entire display "fields" must be developed to generate one "frame", or complete image. For example, the most common rate of 525/60 indicates that:

- There are 525 scanning lines per television frame.

- The field rate is 60 Hz. That is, one television field is developed in 1/60 second.

- Unless specified otherwise, it is assumed that the interlace ratio is 2:1. That is, the frame, a complete image, will be composed of two fields. Therefore, one frame is produced in half the number of scanning lines per frame, in this example 262.5.

Television operation at so-called 1:1 interlace, or non-interlace, is becoming more prevalent. Care must be taken in describing such operation to avoid confusion.

There must be a whole number of scanning lines in each field for 1:1 interlace, whereas to obtain 2:1 interlace each field must have a half line. For example, often it is desired to develop a non-interlace condition for the common 525/60/2:1 interlace system. This may be done by adding a one-half line to the field, resulting in:

	SCAN LINES/ 2 FIELDS	SCAN LINES/ FIELD	FIELD RATE	FRAME RATE
ORDINARY SYSTEM 525/60/2:1 interlace	525	262.5	60 Hz	30 Hz
MODIFIED SYSTEM 1:1 interlace	526	263	59.88 Hz	59.88 Hz

In this instrument, scan rate is selectable over a very wide range by selection of total horizontal line time and the number of scan lines which are to occur in two fields, regardless of the number of fields which make up a frame.

TOTAL HORIZONTAL LINE TIME: Usually the horizontal repetition rate is specified or can be calculated easily. For instance, at the U.S. Broadcast rate of 525/60, the horizontal rate is 15.750 kHz (obtained by multiplying the number of scan lines per frame by the desired frame rate, 525 x 30 Hz). Therefore, the line period, or time required for each line, is 63.492, rounded to 63.5 usec. This time, 63.5 usec., should be selected by keypad entry, resulting in a 15.748 kHz horizontal rate.

SCAN LINES PER 2 FIELDS: Keypad entry for the number of scan lines in two fields is made by entering, for instance, 525 for the 525/60 scan rate. Note that the actual vertical frame rate will be 29.996 Hz, field rate at 59.992 in this example due to the rounding of the total horizontal line time from 63.492 to 63.5 usec.

It is important to obtain exactly particular horizontal and vertical field rates, the master oscillator can be deviated so that the proper frequency can be inserted. The example required rounding of the horizontal line time from 63.492 to 63.5 usec. to accommodate the internal clock rate of 20 mHz. Use of an external clock at precisely 20.002496 mHz will provide a total horizontal line time of 63.492 usec. and a vertical frame of 60 Hz for the example cited on the previous page. If master oscillator deviation is under consideration, contact the factory for further information. Note that deviation for one scan rate may not be appropriate for other rates, and in fact will develop a further offset in their vertical rate.

The format of H drive, V drive and blanking is the same for all rates. The sync waveform can be programmed in any one of six modes according to application requirements. Broadcast, Industrial and Military sync formats have V front porch, V sync and V post equalizing intervals fixed at three lines each. These parameters may be programmed as desired for custom modes, limited only by vertical field length. Refer to Figure 5, page 40, for the Broadcast, Military and Industrial sync formats.

BROADCAST . . The NTSC convention provides 2H rate equalizing pulses for three scanning line intervals (six pulses) before and after the vertical sync interval, 2H rate serrations during the three line vertical sync interval (six pulses), and horizontal front porch as specified in EIA Standard RS-170 and shown as optional in EIA Standards RS-330A and RS-343A.

INDUSTRIAL . . Sync, the same as described under BROADCAST, without equalizing pulses and serrations, per EIA Standards RS-330A and RS-343A.

MILITARY . . Sync which does not include equalizing pulses or serrations, has no horizontal front porch, and no horizontal rate pulse information during the vertical front porch of three scan line duration.

Custom modes allow the user to build his own vertical sync interval not restricted to the three line increments for V front porch, V sync and post equalizing. Three custom V Sync modes are available, Access Codes 4, 5, and 6, for Parameter 16 SYNC FORMAT.

Pulse widths are programmable in 0.1 usec. increments so the waveform can be matched exactly to the desired operating format. Vertical pulse proportions must be synchronous with the horizontal scan lines, and therefore are adjustable but locked to horizontal information to prevent apparent drift or jitter in the display. All pulse widths and pattern proportions should be programmed as required for the rate to be used.

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PROGRAMMING RANGES

Vii television test instruments have been configured for the scanning rate in prevalent use at the present time. Control and calibration ranges have been selected, therefore, to cover timing as appropriate for total horizontal line times of from 10 usec. to 204 usec.; vertical programming ranges are selected to cover a very wide range, including both 50 Hz and 60 Hz field rates, the ones in common use for 2:1 interlaced systems. Therefore instruments can be calibrated for conformance to all EIA standard rates as shown on Table III, page 72, plus other rates that fall outside these timing ranges, both fast and slow scan.

Vii has developed a Proportional pulse standard in which all pulse widths are expressed as a percentage of total horizontal line time. This format, as detailed on Table III, conforms to EIA Standards RS-170 and RS-330, but not exactly to horizontal pulse widths as set forth in EIA Standard RS-343. This format is recommended for all rates, even those higher than 1225/60.

Operation at rates lower than 525/60, higher than 1225/60, and at field rates far removed from 50 or 60 Hz is a special consideration. The test instruments are operable at higher and lower rates; however, there is no precedent for calibration at these rates. Pulse widths as outlined in EIA Standards are not appropriate for very fast or slow scan rates, as a very large percentage of horizontal line time may be lost in blanking, etc. Therefore:

a. instruments will be calibrated to the Vii Proportional Format as outlined on Table III unless other customer specifications are provided;

b. while instruments can operate at quite high rates (including up to 65 kHz horizontal scan) the video signal is limited in maximum repetition rate and rise/fall times. These limitations prevail <u>regardless</u> of rate.

This instrument operates with a universal format for horizontal rate raster development based upon a 0.1 usec. (100 nsec.) timing increment. In this system all horizontal rate parameters, e.g. Total H Line, H Blanking Width, H Front Porch, etc., are programmed to the nearest 0.1 usec. For example, a horizontal line time calculated to be 38.096 usec. (for the 875/60 scan rate) would be rounded to 38.1 usec. The timing difference is minute; the only difference observed would be a slight change in vertical field time. In this example the slightly increased line time would make the vertical field time 16,668.75 usec. (59.9925 Hz vertical field rate) rather than the literal 16,666.66 usec. of a 60 Hz field rate.

TABLE III
Vii "Standard" Scan Rates - Proportional Format

SYNC GENERATOR CHARACTERISTICS - 2:1 INTERLACE

Rate -									
Lines per frame		525	675	729	875	945	1023	1029	1225	625
Lines per field		262.5	337.5	364.5	437.5	472.5	511.5	514.5	612.5	312.5
Field rate		60	60	60	60	60	60	60	60	60
H Rep Rate - kHz		15.750	20.250	21.870	26.250	28.350	30.690	30.870	36.750	15.625
Total H Line - usec		63.5	49.4	45.7	38.1	35.3	32.6	32.4	27.2	64.0
Active H line - usec		52.4	40.8	37.7	31.4	29.1	26.9	26.7	22.4	52.8
Typical Pulse Widths										
4% V Drive	½ TV LINES	21	27	29	35	38	41	41	49	25
V Front Porch	"	6	6	6	6	6	6	6	6	6
V Sync	"	6	6	6	6	6	6	6	6	6
V Post	"	6	6	6	6	6	6	6	6	6
7.5% V Blanking	"	40	50	54	66	70	76	78	92	46
17.5% H Blanking	USEC	11.1	8.7	8.0	6.7	6.2	5.7	5.7	4.8	11.2
10% H Drive	"	6.4	4.9	4.6	3.8	3.5	3.3	3.2	2.7	6.4
2.5% H Front Porch	"	1.6	1.2	1.1	1.0	0.9	0.8	0.8	0.7	1.60
7.5% H Sync	"	4.8	3.7	3.4	2.9	2.7	2.5	2.4	2.0	4.80
3.75% 2H Equalizing	"	2.4	1.9	1.7	1.4	1.3	1.2	1.2	1.0	2.40
7.5% 2H Serrations	"	4.8	3.7	3.4	2.9	2.7	2.5	2.4	2.0	4.80

NOTE: Pulse widths and rates conform to EIA Standards RS-170 and RS-330.
V Blanking nominal pulse width = 1250 usec. at all 60 Hz field rates, nominal 500 usec. for 50 Hz field rates.
V Drive nominal pulse width = 667 usec. at all 60 Hz field rates, nominal 800 usec. for 50 Hz field rates.

TABLE IV
EIA Standard Scan Rates

SYNC GENERATOR CHARACTERISTICS - 2:1 INTERLACE

Rate -									
Lines per frame		525	675	729	875	945	1023	1029	1225	625
Lines per field		262.5	337.5	364.5	437.5	472.5	511.5	514.5	612.5	312.5
Field rate		60	60	60	60	60	60	60	60	60
H Rep Rate - kHz		15.750	20.250	21.870	26.250	28.350	30.690	30.870	36.750	15.625
Total H Line - usec		63.5	49.4	45.7	38.0	35.3	32.6	32.4	27.2	64.0
Active H line - usec		52.5	42.4	38.7	31.0	28.3	25.6	25.4	20.2	53.0
Typical Pulse Widths										
V Drive	T.V.LINES	10.5	13.5	14.5	17.5	18.5	20.5	20.5	24.5	10.5
V Front Porch	"	3	3	3	3	3	3	3	3	3
V Sync	"	3	3	3	3	3	3	3	3	3
V Post	"	3	3	3	3	3	3	3	3	3
V Blanking	"	20	26	28	33	36	39	39	46	20
H Blanking	USEC	11.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	11.0
H Drive	"	6.4	3.5	3.5	3.5	3.5	3.5	3.5	3.5	6.4
H Front Porch	"	1.5	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.5
H Sync	"	4.75	2.75	2.75	2.75	2.75	2.75	2.75	2.75	4.75
2H Equalizing	"	2.35	1.4	1.4	1.4	1.4	1.4	1.4	1.4	2.35
2H Serrations	"	4.5	2.0	2.0	2.0	2.0	2.0	2.0	2.0	4.5

NOTE: Pulse widths and rates conform to applicable EIA Standards RS-170, RS-330, RS-343 and RS-375.
V Blanking nominal pulse width = 1250 usec. at all rates.
V Drive nominal pulse width = 667 usec. at all rates.

Vertical parameters are established in increments of half lines. This conforms to long standing common practice to avoid scanning aberrations which may develop from vertical pulses that are not an integer of horizontal line structure. Raster structure is, universally, based on an even number of scan lines in two fields for non-interlaced scan and an odd number in two fields for 2:1 interlaced systems. Pulses, such as V Blanking, V Drive, V Front Porch and V Sync are configured to the nearest half-line. That is, if V Blanking were specified to be 698 usec. in the example 875/60 scan rate, it would equate to 18.320209 lines, which violates common practice. In the Vii standard system, this would be rounded to 18 lines, resulting in a 685.8 usec. V Blanking pulse width.

The minute differences outlined previously will not be of consequence in nearly all applications. If the shift of vertical field rate is significant due to hum or other effects, the 20 mHz master clock rate can be shifted slightly by use of an external clock slightly off 20 mHz.

Acceptance of the slight deviations as described greatly simplifies the design, construction and programming requirements for raster scan systems. Another advantage is that all scan rates within design operating range can be matched, unlike gaps which are implied in a digital synthesizer system.

While long term common practice and U.S. standards (EIA Standards RS-170, RS-330 and RS-343) have been consistent in the timing of vertical sync interval, deviations have appeared. The Vii standard is consistent with common practice and U.S. standards:

V Front Porch = 3 lines

V Sync = 3 lines

V Post Equalizing = 3 lines

Serrations @ 2H rate

Equalizing pulses @ 2H rate

The leading and trailing edges of V Blanking and V Drive are coincident with timing of the leading edge of H Blanking. The leading and trailing edges of V Sync are coincident with timing of the leading edge of H Sync.

Should there be an application which demands absolute timing conformance, the universal time base system may not apply. However, these applications can be satisfied with a customized system dedicated to that particular use. A technical note is available from Vii, "Structure of the Television Raster", which is a thorough discussion of all factors that influence structure and timing of the raster scan technique.

PROGRAMMING AND USER CODES

The following review of operator instructions defines all modes of operation, error messages, and parameter definitions relevant to the Model 2501. Flow charts detailing all operating procedures of the instrument are also included. These programming and user codes will serve as an aid in operating the Model 2501.

Raster structure is established by keypad entry of individual timing parameters for each raster desired, in the range of from 10 kHz to 100 kHz horizontal rate at various numbers of scan lines per field and vertical field rates. Horizontal sync and pattern parameters may be entered in 0.1 usec. timing increments; vertical parameters are entered in increments of 0.5 t.v. lines. Storage is provided for up to 69 separate raster structures. The operator may build a rate, each parameter at a time, or may choose standard proportion and format which will be computed automatically. Scan rates may be stored, recalled for use, edited or deleted by keypad code entries. Software "lock-out" is provided to prevent unauthorized editing without proper security password. All software functions (build, edit, recall and the security password) are conducted as shown on flow charts found later in this section.

RASTERS 1 THROUGH 69

The Model 2501 contains a permanent "default" scan rate, Access Code 99, which is stored in inaccessible memory. This rate is 525/60, per EIA Standards RS-170 and RS-330A. It will appear whenever power is applied to the instrument, and cannot be erased or edited. No other scan rate can be stored in this memory location. RATE 99 parameters may be edited (changed) for temporary use but cannot be stored in the RATE 99 memory location; the revised parameters can be transferred for storage in another memory location.

The generator has been tested at the factory with several scan rates as itemized in the RasterMaster Log. These rates have been chosen to fully exercise the system and demonstrate various features of the computerized sync generation system. Special features of these rates are detailed on temporary RASTER SUMMARY forms included in the Log. These RASTER SUMMARY forms should be discarded if other scan rates are stored in the specified memory location. Any one of these scan rates can be deleted. Refer to FLOW CHARTS for proper procedures.

RCL (RECALL)

RECALL generally finds the requested raster number and puts it in the running state. Only one prompt is used in RECALL (RASTER NUM). The only way to exit this mode other than by entering a raster number is by pressing the RCL key a second time; the raster currently in use will be displayed.

RECALL has two dedicated sub-modes. If, when the RASTER NUM prompt is displayed, the user enters a decimal point (.), and the mode is switched to search. If the user enters .1 (decimal point and "one"), then mode is switched to LIST. Both of these routines are detailed in the TO SEARCH FOR A RATE PREVIOUSLY STORED (page 85) and TO REVIEW ALL RATES IN STORAGE (page 86) flow charts.

In the search mode, the system locates all rasters which the user has entered with the requested number of scan lines in two fields. The system displays the number of lines, field rate, and raster number for the first match encountered. If no match is found, it states NOT FOUND. To view the next match, a decimal point must be entered followed by ENTER. If no more matches are found, then LAST ENTRY is displayed. At that point, the search/recall mode is terminated. If the user wishes to run a rate when it is displayed during the search mode, simply press ENTER and the rate is loaded and search is terminated.

In the list mode, stored rates are displayed in sequence. It automatically starts with raster number one and sequences through all of the rasters each time the operator presses the decimal point (.) and ENTER.

To exit either search or list at any time, simply press RCL.

SECURITY PASSWORD→ 719 ENTER

The user cannot access the BUILD (BLD) or EDIT (EDT) modes unless a security password is entered. This safeguard prevents unauthorized entry, alteration, or deletion of information in storage. Two passwords may be used - either the primary password, or secondary password. The primary password is factory installed and cannot be changed. The secondary password is user programmed and can be altered as often as the user wishes.

TO ACCESS THE EDIT (EDT) OR BUILD (BLD) MODES

1. Enter either the primary or secondary password. Note that this step is not displayed.

2. Press the ENTER key. Note that this step is not displayed.

3. To check access, press either the BLD or EDT key. The corresponding red LED indicator light should light, indicating access.

4. Press the BLD or EDT key again to exit the mode. Note that these modes remain accessible until access is removed as noted below. Access is lost automatically whenever power is removed from the unit.

TO REMOVE ACCESS TO THE EDIT (EDT) OR BUILD (BLD) MODES

1. Enter either the primary or secondary password.

2. Press the ENTER key.

3. To check non-access, press either the BLD or EDT key. The LED indicator should not light, indicating that there is no longer access to these modes.

- OR -

1. Turn the instrument OFF.

2. Wait at least ten seconds.

3. Turn the instrument ON.

4. Wait at least ten seconds.

5. To check non-access, press either the BLD or EDT key. The LED indicator should not light, indicating that there is no longer access to these modes.

TO INSTALL THE SECONDARY PASSWORD

1. Nothing shows on the display for this sequence, so care should be taken to avoid an erroneous code entry. If the secondary password does not appear to work, repeat the entry as described above.

2. Enter the primary password, plus a decimal (.) point.

3. Press the ENTER key.

4. Press the desired secondary password, up to four digits.

5. Press the ENTER key.

6. Check access and removal of access to the BUILD or EDIT modes as outlined above.

7. To change the secondary password, repeat steps 1 through 4. Entry of new secondary password digits will automatically "overwrite" a secondary password installed previously.

BLD (BUILD)

BUILD is used to develop a raster from scratch. Each parameter must be entered individually except that on the PROP sync and H PATTERN prompts for which the values are automatically calculated to the Vii Proportional Format. The BUILD mode is essentially a sequential operation except when proportional is requested. The logical conclusion to the BUILD mode is to save the developed raster, but you are not required to permanently store (save) it. To allow the newly built raster to run without permanently storing it, simply answer "no" (Ø) when the SAVE IT? prompt is encountered.

Since the BUILD mode is sequential, there must be a way to back up to correct a previously entered value. This is accomplished by entering a decimal point (.) without a number, then press ENTER for each back-up step desired. This will also allow you to examine the proportional calculations before saving the format.

The BUILD mode may be exited by pressing the BLD button a second time. Data entered to this point will be erased; operator reverts to the previously used raster.

EDT (EDIT)

EDIT is used to examine and, if desired, modify an existing format. If modified, it can be saved as a new raster number, old raster number, or not saved at all. There are many conditions under which the user may enter the EDIT mode.

If the format you wish to edit is already running, press EDT. Then when the RASTER NUM prompt appears, press Ø and then ENTER; the edit mode becomes immediately interactive. Each parameter will be changed at the outputs when a new value is entered.

The EDIT mode may be exited by pressing the EDT button a second time. Revisions will be retained temporarily but not stored.

Another way to enter EDIT is to request a raster number other than the one running. Press EDT, enter raster number desired, and press ENTER. For example, raster number 29 (875/60) is running and the user wishes to review raster number 33 (1225/60). In this situation, 875/60 will continue to run while 1225/60 is being examined. But as soon as any parameter is changed, the 1225/60 format will begin to run. If the user wishes to examine 1225/60 but not to run it, then as the requested parameter is displayed he must depress ENTER without making any numerical changes. In this way, the user can check one format while running another. Note that raster numbers referred to for this 875/60 and 1225/60 scan rates are only examples.

EDIT is essentially a two-step process. After the desired raster number is keyed in and entered, it requests the code number for the parameter to be examined. Refer to PARAMETER DEFINITIONS (page 83). After the parameter is entered, it displays the old value and waits for the new value to be keyed in. Once the new value is keyed in, press ENTER or, if no revision is desired, simply press ENTER only. This brings the procedure back to requesting the parameter desired next.

The EDIT mode can be used to modify parameters of RATE 99 on a temporary basis, but will not insert changes to this pre-programmed raster structure.

CORRECTION OF ENTRY ERROR

If an incorrect number is entered, it may be erased by entering a series of zeros ("Ø"). When the display returns to zero at all digit locations, the correct number may be entered.

RASTER STORE

Saving the raster format is a normal completion of the BUILD or EDIT mode. When the SAVE IT? prompt is displayed, one may enter a "yes" (1) or "no" (Ø). If yes, then OVERWRITE is displayed. At this point, one of two choices can be made. If no, then the "save" sub-mode is exited. If yes, then WAITING is displayed. At this point again, one of two choices can be made. If any key on the pad is pressed, the save mode will be exited. If the FORMAT STORE button to the left of the keypad is pressed, then WORKING is displayed and approximately one second later, the raster format is in storage and will be displayed.

RASTER DUPLICATION WITH A NEW ACCESS CODE

An existing raster can be transferred to a new memory location and then may be edited (modified) as required. This prevents having to totally build a raster with only minor variation from an existing stored raster structure.

1. Access the EDIT (EDT) mode for the raster now in storage:
   Press EDT
   Enter raster access code
   Press ENTER

2. The display will read PARAMETER?.
   Enter parameter 34
   Press ENTER
   Enter new access code desired
   Press ENTER

3. The display will once again read PARAMETER?. Other editing may be performed by requesting appropriate parameter numbers as shown on the flow chart. Refer to PARAMETER DEFINITIONS (page 83).

4. When all edit revisions have been entered, perform storage routine as shown on the flow chart (page 88). The edited raster will be stored in the new access code memory file; the original raster will remain in its memory file without change.

FIELD RATE INDICATION

All field rates below 99.9 Hz are rounded to tenths. All field rates between 100 and 999 Hz are rounded to integer values only; no decimals are displayed. For all field rates greater than 999 Hz, no calculation is made and three asterisks (***) are displayed where field normally appears.

SYNC FORMAT

Sync format (Parameter 16) can be programmed in any one of six modes:

1 = standard BROADCAST format
2 = standard INDUSTRIAL format
3 = standard MILITARY format
4 = Custom A (BROADCAST format only)
5 = Custom B (INDUSTRIAL format only)
6 = Custom C (MILITARY format only)

Standard Broadcast, Industrial and Military sync formats (1, 2 and 3) have V front porch, V sync and V post equalizing intervals fixed at three (3) lines each. These parameters may be programmed as desired for Custom A, B and C modes (4, 5 and 6) limited only by vertical field length.

ERROR MESSAGES

HELP I AM BROKE . . a catastrophic error has occurred; usually a hardware failure found during a self check, but could also be caused by a previously untrapped operator error. The latter can be cleared by resetting the system (power off-on cycle).

HELP IT IS BROKE . . same as above.

INVALID ENTRY . . incorrect mode switching while attempting to exit. To correct, depress the selected mode again.

OVERWRITE . . trying to save in a previously occupied raster number. Answering with a "yes" (1) will overwrite the existing format while answering "no" (Ø) will cause an exit from save.

BAD WRITE . . normally means that storage facility is defective or the particular position is defective. If a save attempt at another raster number fails, the storage components or a board may need to be replaced by the factory.

NOT IMPL . . no raster is implemented (stored in that particular memory location). This message is used only in the LIST (REVIEW ALL RATES IN STORAGE) mode.

E1 . . too many decimal places. The time base is limited to one decimal place (1/10 usec.).

E2 . . entry out of range.

E3 . . entry under range.

E4 . . incorrect operator command, such as answering with with a 2 for "yes" or "no" answer.

ERROR MESSAGES (cont.)

E5 . . attempting to recall an unimplemented raster number.

E6 . . same as E5 but under different conditions.

E7 . . reserved parameter number.

E8 . . decimal point in a half-line entry.

NOTE: One may recover from E1 through E8 by entering a new value for the operation in process.

W1 . . invalid standard broadcast sync mode.

W2 . . invalid standard industrial sync mode.

W3 . . invalid standard military sync mode.

W1 and W2 conditions are identical, requesting Broadcast or Industrial sync modes without a horizontal front porch. W3 occurs when requesting Military sync with a horizontal front porch.

To circumvent these conditions, the user must choose one of the three custom modes - CST4 for broadcast, CST5 for industrial, or CST6 for military. This enables the user to implement front porch as desired for any v sync mode.

PARAMETER DEFINITIONS

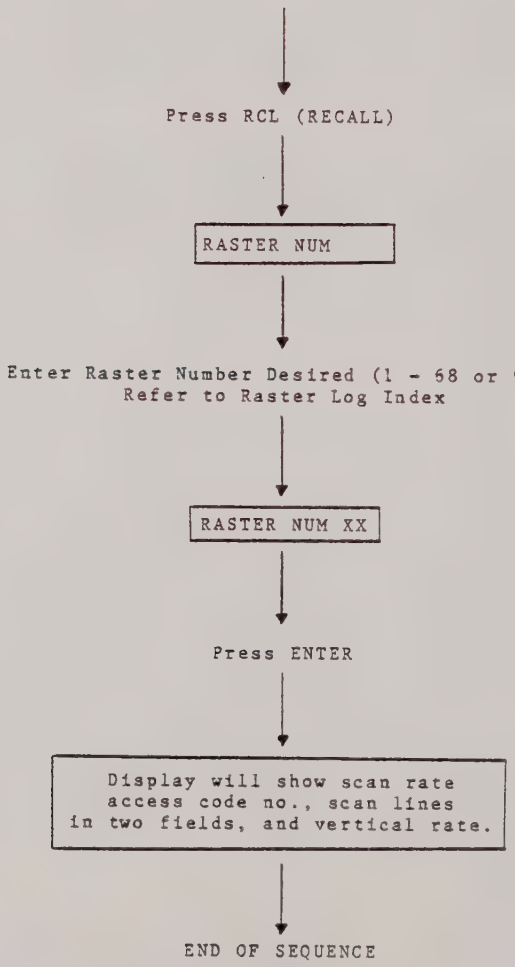
Parameter Number	Display Message	Description
1	NO. LINES	number whole lines in 2 fields
2	H LINE TIME	horizontal line time (1/10 usec)
3	PROP/CUST	proportional = 1, custom = Ø pulses
4	H BLANKING	horizontal blanking (1/10 usec)
5	H FRNT POR	horizontal front porch (1/10 usec)
6	H SYNC	horizontal sync (1/10 usec)
7	2H SERR	2H serrations (1/10 usec)
8	2H EQUAL	2H equalizing (1/10 usec)
9	H DRIVE	horizontal drive (1/10 usec)
10	H TRIG PH	horizontal trigger phase (1/10 usec)
11	H TRIG WID	horizontal trigger width (1/10 usec)
12	V BLANK	vertical blanking (1/2 lines)
13	V DRIVE	vertical drive (1/2 lines)
14	V TRIG PH	vertical trigger phase (1/2 lines)
15	V TRIG WID	vertical trigger width (1/2 lines)
16	SYNC FORMAT	sync format: 1 - 6
17	V FRNT POR	vertical front porch (1/2 lines)
18	V SYNC WID	vertical sync (1/2 lines)
19	V POST WID	vertical post (1/2 lines)
20	H PATTERN	horizontal pattern: 1 = standard Ø = custom
21	V BAR POS	vertical bar position (1/10 usec)
22	V BAR SPC	vertical bar spacing (1/10 usec)
23	H WIN START	horizontal window start (1/10 usec)
24	H WIN STOP	horizontal window stop (1/10 usec)
25	H BAR POS	horizontal bar position (1/2 lines)
26	H BAR SPC	horizontal bar spacing (1/2 lines)
27	V WIN START	vertical window start (1/2 lines)
28	V WIN STOP	vertical window stop (1/2 lines)
29	reserved	
30	reserved	
31	reserved	
32	APL START	average picture level start
33	APL STOP	average picture level stop
34	RASTER NUM	raster access number

FLOW CHARTS

The following are flow charts detailing proper operating procedures of the Model 2501. Some short cuts in the routines are possible, but remember that they are not factory approved and may create secondary problems. It is recommended that sequences be followed as detailed on flow charts.

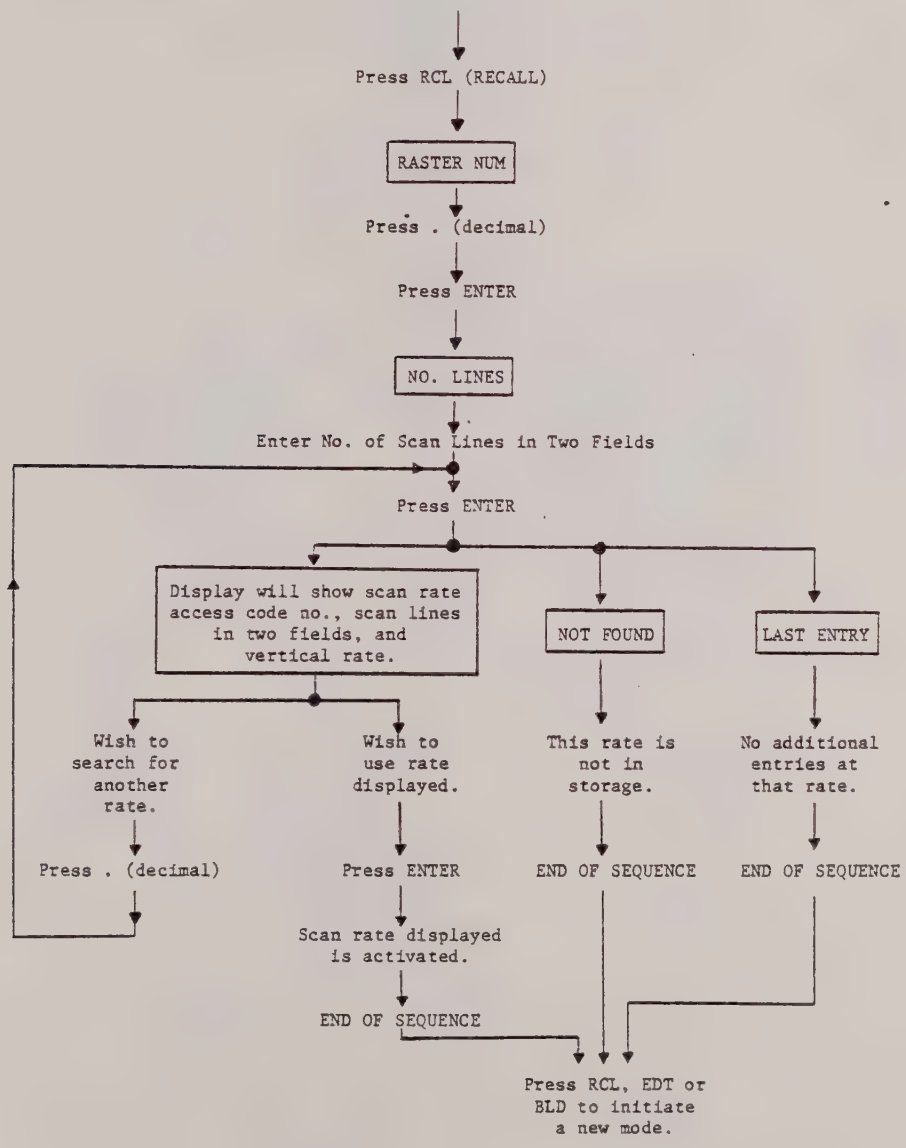
TO RECALL A RATE PREVIOUSLY STORED

When power is applied to the instrument, RATE 99 (525/60 scan rate per EIA Standard RS-170, Broadcast format) will appear. This initial rate is permanently programmed and cannot be altered. The instrument will return to this rate whenever power is interrupted. Signals at this rate automatically appear at output connectors.



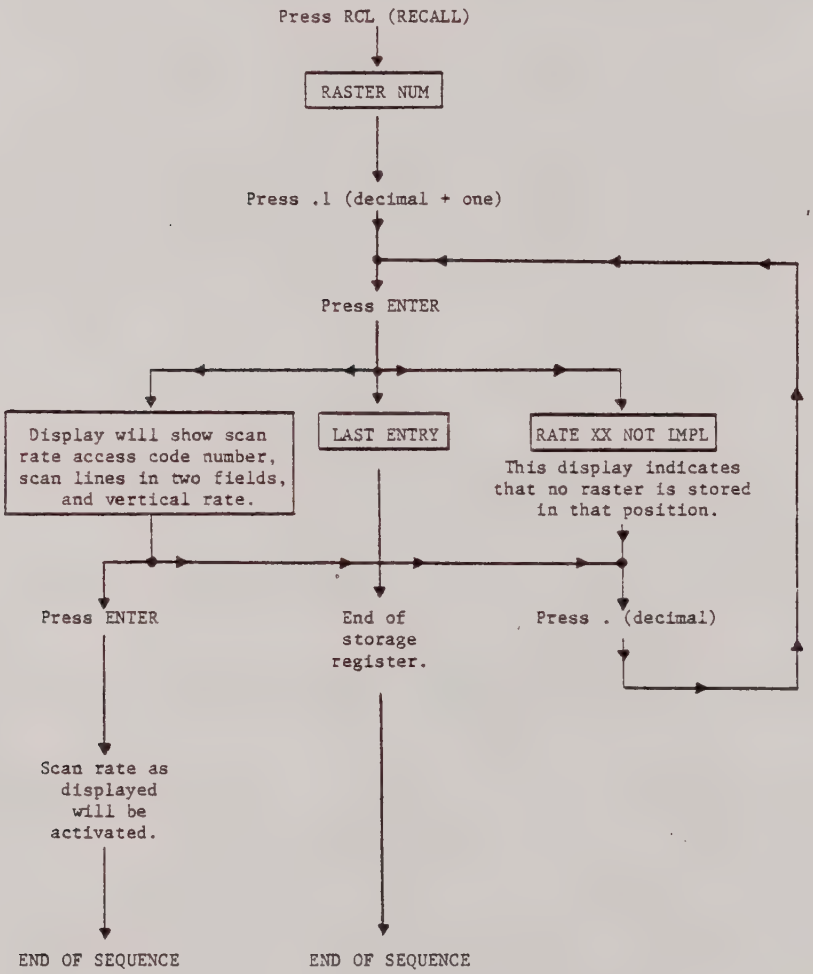
TO SEARCH FOR A RATE PREVIOUSLY STORED

This mode allows the user to survey all rasters which may be in storage for any particular number of scan lines in two fields. For instance, there could be 875/60 Broadcast format, 875/60 Industrial format, 875/50 and 875/37.6. The user can inspect each one to verify Raster Summaries as follows:

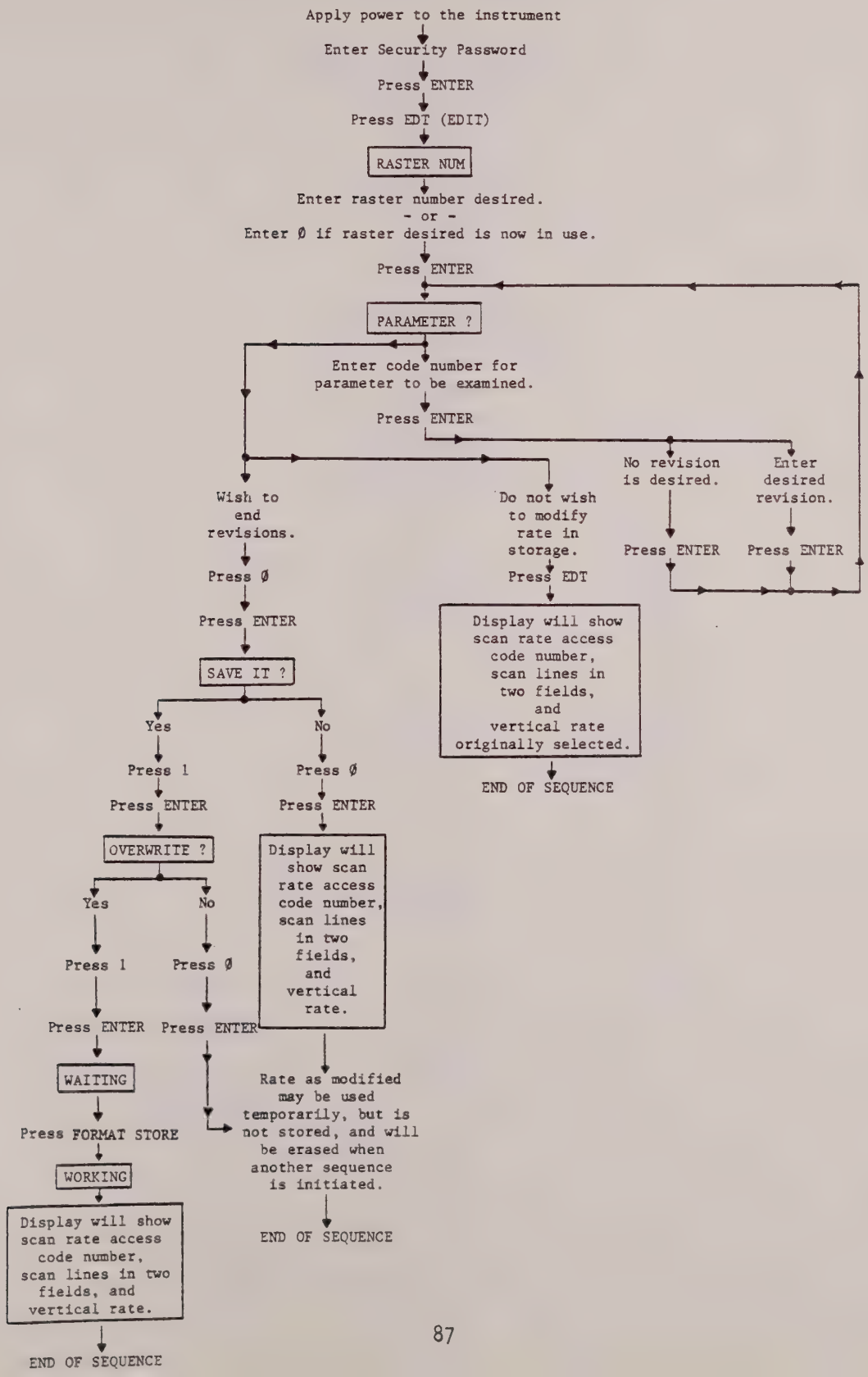


TO REVIEW ALL RATES IN STORAGE

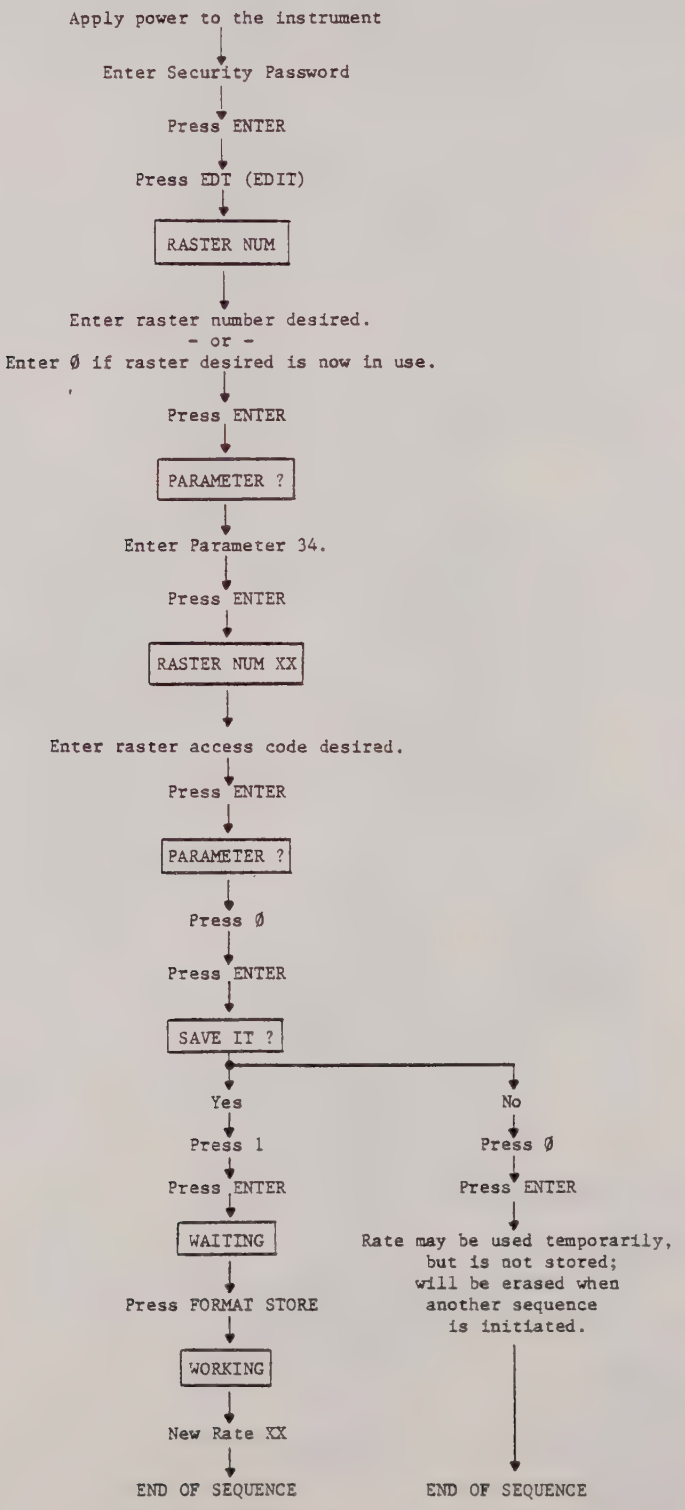
The operator may exit this mode at any time by pressing RCL (RECALL). The rate last in use will be displayed. Output signals continue to be generated at the last rate in use during review sequence.



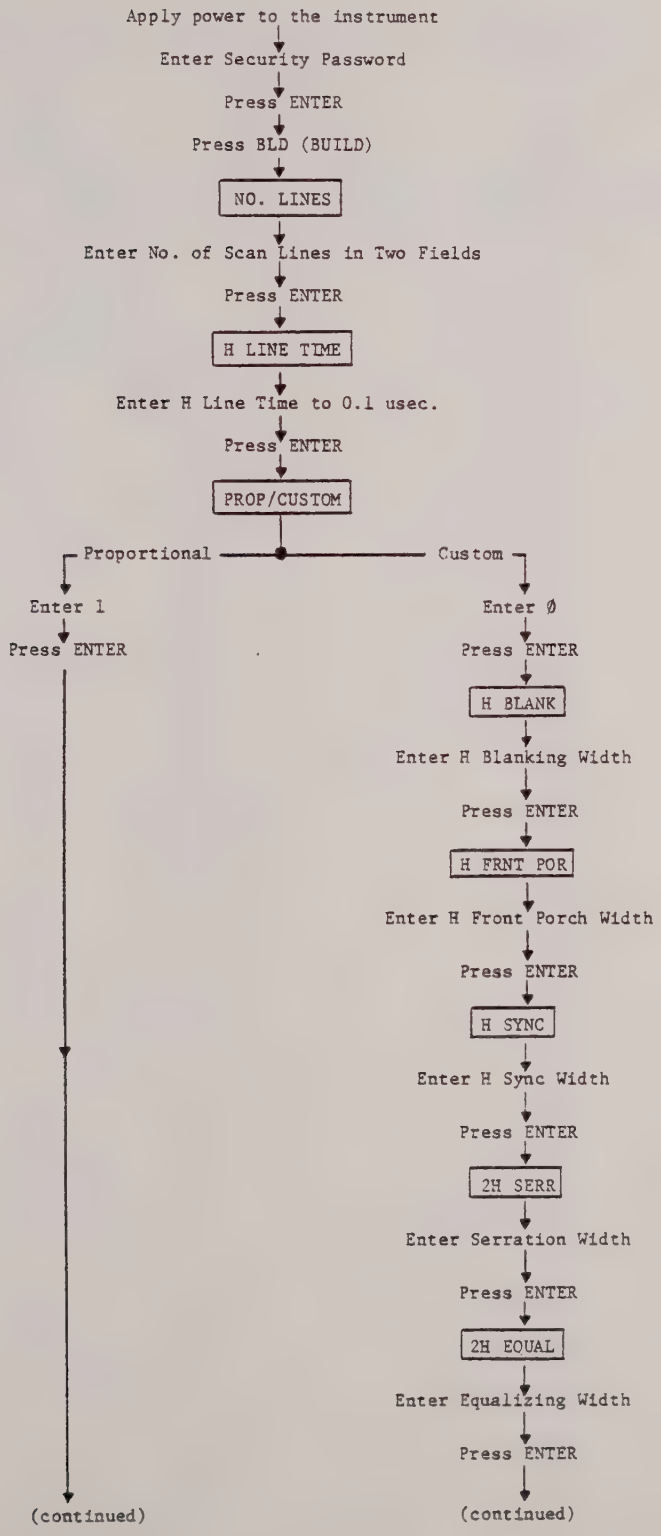
TO EXAMINE OR EDIT (MODIFY) PARAMETERS IN A SCAN RATE PREVIOUSLY STORED

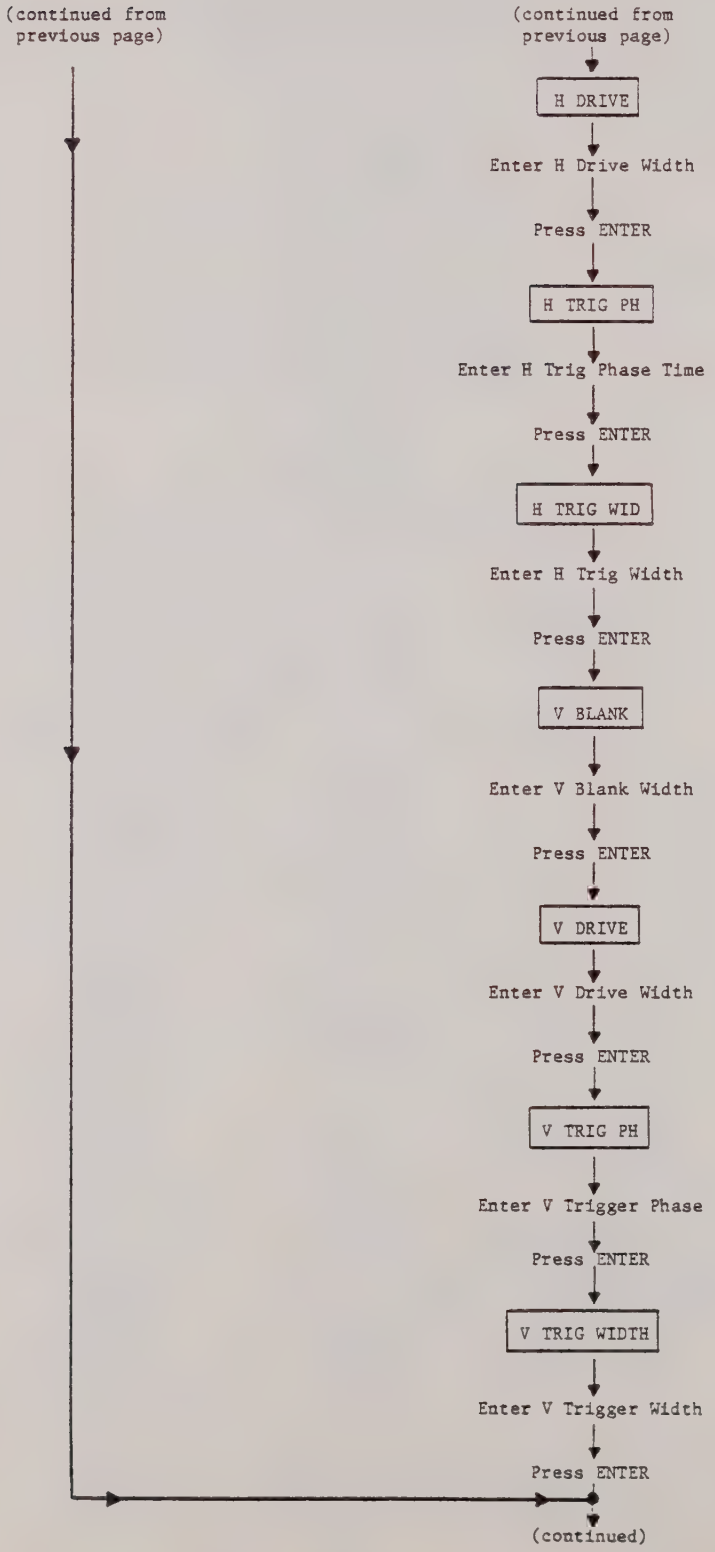


RASTER DUPLICATION WITH A NEW ACCESS CODE

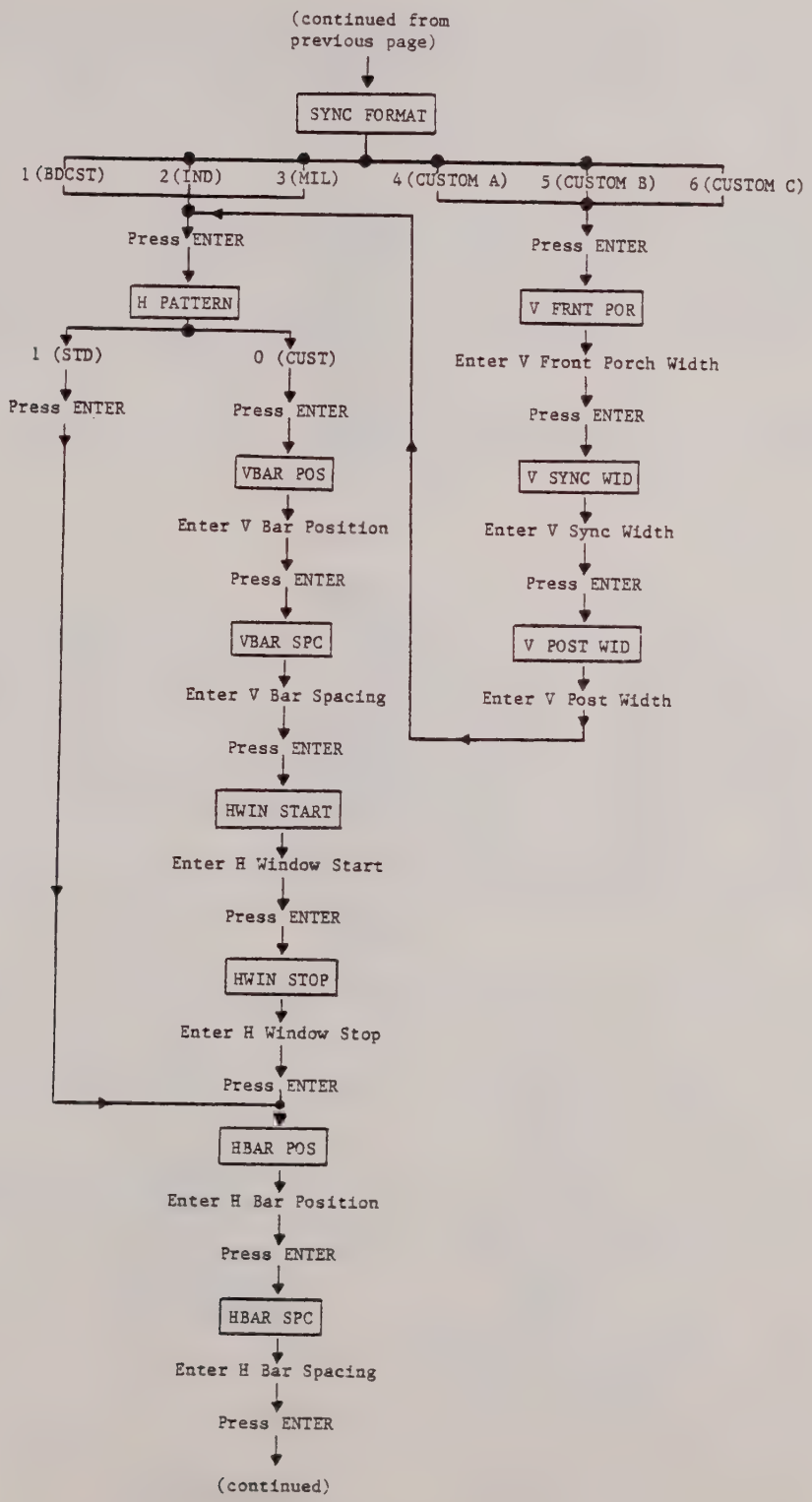


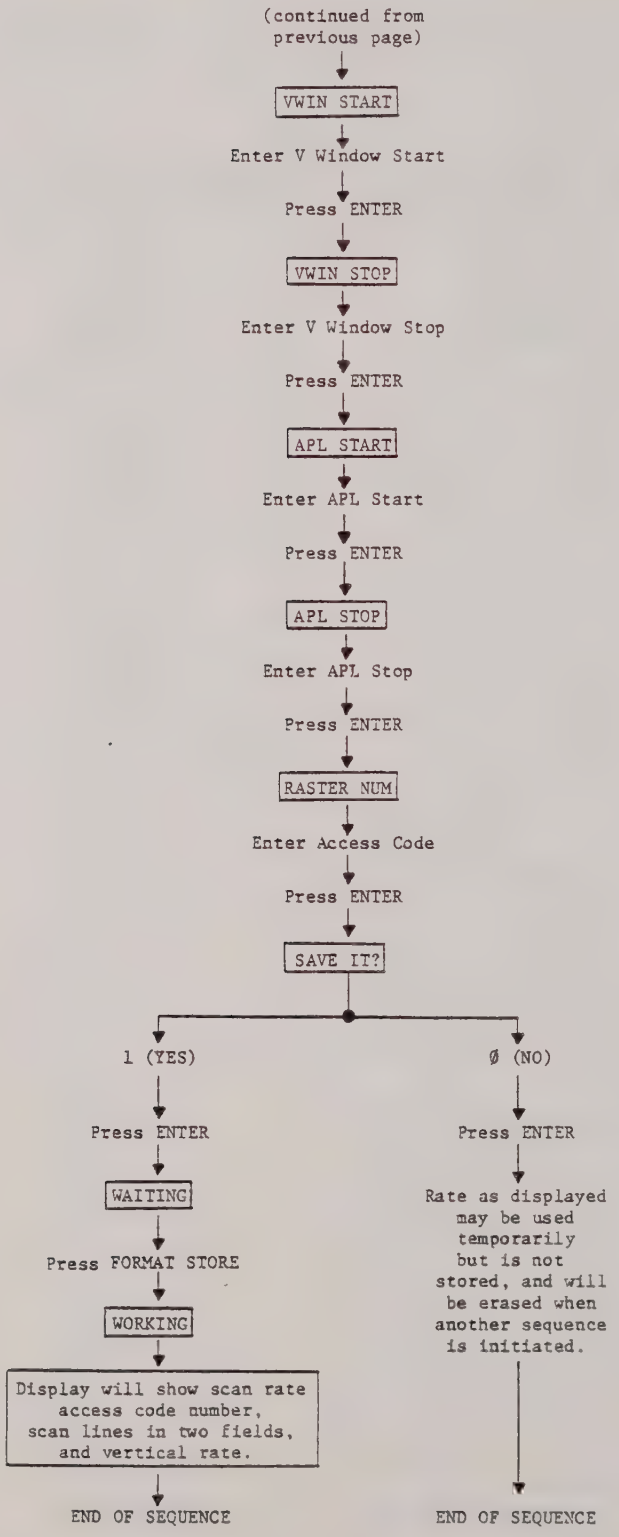
TO BUILD A NEW SCAN RATE




(continued from previous page)
(continued from previous page)
H DRIVE
Enter H Drive Width
Press ENTER
H TRIG PH
Enter H Trig Phase Time
Press ENTER
H TRIG WID
Enter H Trig Width
Press ENTER
V BLANK
Enter V Blank Width
Press ENTER
V DRIVE
Enter V Drive Width
Press ENTER
V TRIG PH
Enter V Trigger Phase
Press ENTER
V TRIG WIDTH
Enter V Trigger Width
Press ENTER
(continued)

TO BUILD A NEW SCAN RATE (cont.)




(continued from previous page)
VWIN START
Enter V Window Start
Press ENTER
VWIN STOP
Enter V Window Stop
Press ENTER
APL START
Enter APL Start
Press ENTER
APL STOP
Enter APL Stop
Press ENTER
RASTER NUM
Enter Access Code
Press ENTER
SAVE IT?
1 (YES)
Press ENTER
WAITING
Press FORMAT STORE
WORKING
Display will show scan rate access code number, scan lines in two fields, and vertical rate.
END OF SEQUENCE
Ø (NO)
Press ENTER
Rate as displayed may be used temporarily but is not stored, and will be erased when another sequence is initiated.
END OF SEQUENCE

PERFORMANCE VERIFICATION

Vii test equipment operates automatically, developing an analog television signal through digital techniques. Therefore, no extensive calibration procedure is required. The procedure outlined below should be followed to ascertain that the instrument is functioning properly and that pattern and pulse values are proper for the scan rate in use.

This procedure is dual purpose. It is used to verify performance of the instrument to specification, a procedure which can be accomplished without removal of covers and change of internal controls. If change is desired, such as to change signal levels, or is indicated by variations observed during performance verification, the top cover must be removed for access to controls. Control locations are described under FRONT PANEL CONTROLS (page 25) and INTERNAL CONTROLS (page 33).

Steps to be completed for a signal change are marked by an asterisk (*); these steps do not need to be considered for performance verification only.

Equipment

1. Any good, general purpose oscilloscope with adequate high frequency response is suitable for inspection of the waveforms. Calibration of the Model 2501 requires an oscilloscope response that is flat (±0.5 db) to greater than 30 mHz to show complete detail of risetime. Direct coupling (d.c.) is preferred to prevent a false appearance of a tilt on the video waveform at vertical rate. The oscilloscope should have provisions for external synchronization from either horizontal or vertical drive to view the composite video output waveform with convenience. Also, a delaying sweep capability will permit inspection of selected horizontal lines within the vertical television field. Typical instrumentation suited for this use would be the Tektronix Type 2465 or equivalent.

2. A television monitor capable of displaying the test signal such as Dage-MTI Model HR2000 (monochrome) or Conrac Model 7211 (RGB color).

3. A UG-274/U BNC series coaxial cable tee and 75 ohm termination; Dage 540-2 or equivalent.

4. A minimum of two coaxial cables, RG59B/U, no more than three feet in length with BNC connectors.

5. An accurate voltmeter, ±1% accuracy at least 10,000 ohms per volt impedance, 0 - 10v. range.

6. A frequency counter capable of indicating horizontal and vertical repetition rates, such as the Fluke Model 1900A or equivalent. If available, a counter with dual inputs and the capability for external clocking, such as the Monsanto Counter-Timer, Model 100B will be useful.

Tolerances have not been standardized in the television industry and often vary according to particular system requirements. Therefore, adjustments called out herein are described without specific tolerance range. Pulse width settings are observed on an oscilloscope display, in which close setting is a matter of technician care in procedure. In factory calibration a tolerance of ±5% is assumed as a maximum allowance on all oscilloscope measurements, i.e. a pulse width of 10 usec. must be within ±0.5 usec. to be considered acceptable. The horizontal scan rate is derived from a crystal oscillator in which case a repetition rate tolerance of 0.01% can be assumed unless specified otherwise.

Voltage Levels

* If there is any deviation from specified signal level ranges or a malfunction, power supply levels must be verified prior to conducting the performance verification procedure (+12v., +5v., +8v. and -5v.) to establish proper reference levels for all operations. Test points are provided on the POWER REGULATOR circuit card as shown on Drawing L-2110 to check the voltage levels. A control is provided at the right side of the POWER REGULATOR card to adjust the +5v. supply. Others are not adjustable. The computer section operates from a dedicated +5v. switching power supply which is not accessible for routine test.

Measurement Conditions

a. A 10 usec. per division oscilloscope sweep rate is suggested for 525-line scan rate when observing horizontal information. Any convenient sweep rate which will show the entire horizontal line may be used for other rates.

b. The 2 msec. per division sweep rate is suggested to observe vertical information for all EIA Standard scan rates and others which have a 60 Hz field rate. The 5 msec. per division sweep rate is suggested for vertical frame observation. Other convenient rates may be used for television formats having other than a 60 Hz field repetition rate. Be sure that more than a full field is visible on the oscilloscope screen for proper vertical rate pulse inspection.

c. The use of Delayed oscilloscope sweep is quite helpful in viewing detail of vertical rate waveforms. Care must be taken in setting up the oscilloscope, however, to obtain a clear and accurate waveform.

1. The oscilloscope main sweep should be synchronized from a vertical rate pulse. External scope sync to V Drive is preferred, although the "TV Field" sync offered in some oscilloscopes may be adequate.

2. The main (A) sweep must be set to a sweep rate which displays more than one field. For example, the 2 msec. per division sweep rate is suitable for a 60 Hz field rate. A slower sweep, such as the 5 msec. per division, would be required for a 50 Hz field rate. This prevents a "strobing" effect which appears as a timing error in an interlaced television signal.

3. Delayed (B) sweep is, preferably, externally synchronized from a horizontal rate signal, such as H Drive. Internal B sweep sync is possible with a composite video signal. A setting such as "B Starts After Delay" is useable, but the horizontal rate waveform may show some jitter.

4. The operating sequence is as follows, after connections are made:

   a. View the full vertical field with Sweep A. Verify that more than one full field is displayed.

   b. Select "A Intensified by B" sweep mode. This indicates the part of the field which will be displayed by the B sweep.

   c. Select the B sweep length required to inspect the position of the field of interest.

   d. Select B sweep to view the desired portion of the vertical field.

Performance of the programmable sync generator section must be verified using the following procedure prior to test of the pattern generator section. Connect the generator for use as described in the CONNECTIONS (page 17) section of this manual.

Before proceeding with the following performance verification procedure, it is essential to be familiar with various programming modes which will be referred to. It is recommended that the user review the PROGRAMMING AND USER CODES section (page 75) thoroughly before proceeding. All modes of operation, error messages, parameter definitions and flow charts are detailed and will serve as an aid in operating the Model 2501.

Typical Test Procedure

This test procedure is written for the 525/60 scan rate and is an example applicable to all scan rates and operating modes. The procedure which follows is to be used with an oscilloscope to check the instrument output obtained from any programming operation, whether to build, edit or to recall information previously stored.

Timing values shown in parenthesis () are what should be measured for the 525/60 "default" scan rate, Access Code 99. All timing value increments are programmed in 0.1 usec. increments. However, there are certain processing delays which may cause some slight shift in signals. All oscilloscope measurements should match the displayed, programmed value within ±10%.

1. When power is applied to the Model 2501, the unit will display RATE 99 525/60.0. If another rate is desired, enter the appropriate access code number. (Enter the security password) so that various parameters may be examined. Enter the edit (EDT) mode so that individual parameters may be examined (refer to page 79).

2. Sync the oscilloscope from the leading edge (-) of H Drive. Set oscilloscope sweep rate as desired for inspection of timing as described in each step of adjustment (10 usec. per division for RATE 99).

3. Observe the H Drive waveform at the rear panel. Pulses should be 8 volts, pk-pk (unterminated) negative going with leading edges spaced as shown on Table III (page 72) for the various scan rates representing total horizontal line time (63.5 usec. for RATE 99). (Enter Parameter No. 2,) H LINE TIME, and compare displayed value to oscilloscope measurement. Check the H Drive pulse width; enter Parameter 9, H DRIVE, and compare displayed value to oscilloscope measurement (10% of the total line time, 6.4 usec. for RATE 99).

4.* Synchronizing pulse amplitude is adjustable over a nominal range of 3.5v. to 4.5v. pk-pk when outputs are properly terminated. Adjust the output pulse amplitude as desired, usually to 4.0v. pk-pk using the control at the right side of the PULSE OUTPUT circuit card (Position 11C, L-2003). Note that this control provides simultaneous adjustment to all four outputs: H Drive, V Drive, Blanking and Sync.

5. Sync the oscilloscope from the leading edge (-) of V Drive. Set oscilloscope sweep to 2 msec. per division. Observe the V Drive waveform.

   The V Drive pulses should be spaced 16,667 usec. apart, occurring at a 60 Hz rep rate for RATE 99. Switch oscilloscope sync to LINE; the pattern should either be stationary or drift very slowly to the right or left. A rapid travel or apparently out of sync signal indicates that the vertical rate is incorrect, due to improper master oscillator frequency or improper line count. Note that this test cannot be made for rates not developing a 50 Hz field, such as the 625/50 rate, where the field rep rate is not the same as the power line frequency. Return oscilloscope sync to V Drive.

   Connect the frequency counter to the V Drive output to verify repetition rate (nominally 60 Hz, for RATE 99).

   Select Parameter 1, NO. LINES, which indicates the number of scan lines in two fields; compare to the displayed value.

   If an electronic counter with dual inputs is available, it can be used to count the number of scan lines per field. Connect H Drive to the Channel A (Ext Clock) input and V Drive to the Channel B (Gate) input. Select counter function to read the number of lines which will occur in the interval between V drive pulses (262.5 for RATE 99).

6. Expand oscilloscope sweep rate as necessary to measure width of the V Drive pulse. Enter Parameter No. 13, V DRIVE, to display the programmed value. This pulse is programmed in "half-lines"; pulse width must be computed - NO. HALF LINES ÷ 2 x TOTAL H LINE TIME - and compared to measured value (for RATE 99 the V Drive pulse width is 21 half lines ÷2 = 10.5; 10.5 x 63.5 = 666.75 usec).

7. Observe the Blanking output, with oscilloscope sync at H Drive. Observe amplitude, polarity and leading edge spacing to be as described previously. Check H Blanking pulse width (11.1 usec. for RATE 99). Enter Parameter No. 4, H BLANKING, and compare displayed value to oscilloscope measurement.

8. Sync the oscilloscope from the leading edge of V Drive, and set sweep rate at 2 msec. per division for inspection of the vertical rate blanking waveform. The vertical blanking intervals should be spaced 16,667 usec. apart, occurring at a 60 Hz rep rate for RATE 99. Enter Parameter No. 12, V BLANK, to display the programmed value. Width of the vertical component of blanking is in "half-line" increments. Use expanded or delayed oscilloscope sweep to measure V Blanking interval width. Compute the programmed width - NO. HALF LINES ÷ 2 x TOTAL H LINE TIME - and compare to measured value. (For RATE 99, the V Blanking interval is 40 half lines ÷ 2 = 20; 20 x 63.5 = 1270 usec).

9. Sync oscilloscope to the leading edge (-) of V Drive. Set oscilloscope sweep at 2 msec/div. Observe the Sync output and inspect for proper vertical sync waveform using either expanded or delayed sweep. Enter Parameter 16; the display should read "SYNC FORMAT BCST" for Rate 99. The Broadcast sync format is permanently programmed in the default 525/60 scan rate. For other rates, any one of six vertical sync formats may be indicated:

BCST . . standard Broadcast (selector code 1)
IND . . standard Industrial (selector code 2)
MIL . . standard Military (selector code 3)
CST4 . . custom Broadcast (selector code 4)
CST5 . . custom Industrial (selector code 5)
CST6 . . custom Military (selector code 6)

Compare the oscilloscope waveform to the proper format shown in Figure 5 and described on page 68. The standard formats always have V front porch and V sync widths equal to the time of three horizontal lines (entered as six half-line increments), whereas custom modes may have other vertical widths.

If BCST sync format is not indicated, press 1 (one) and ENTER to select the BCST format. Inspect the vertical sync interval closely, noting presence of six positive serrations in the V sync interval (from 3H to 6H past V drive leading edge, from 191 usec. to 382 usec. at RATE 99). It may be necessary to expand the sweep for this observation; delaying sweep at approximately 50 usec/div. also will permit convenient viewing of the V sync interval. Six serration pulses should be present in the V sync interval (occurring at 2H rate). Observe that six equalizing pulses are present before and after the V sync interval, also at 2H rate.

Enter the INDUSTRIAL format by selecting "2" after Parameter 16, SYNC FORMAT, has been entered. This sync format provides no serrations or equalizing pulses, leaving the waveform as shown in Figure 5, page 40.

Enter the MILITARY format by selecting "3" after Parameter 16, SYNC FORMAT, has been entered. For RATE 99 and other rates which have the H front porch other than zero, the display will show error code W3, as the standard Military format requires H front porch to be 0 usec., an unallowable condition. A change of H front porch to zero is inhibited in the EDIT mode.

The three custom Sync Format modes allow complete flexibility in waveform manipulation, circumventing the error trap encountered above. Enter Sync Format 6; the display will read SYNC FORMAT CST6. The waveform should be the Military format as shown in Figure 5 except that the H front porch will be as previously entered, not zero. Select Parameter 5, H FRONT PORCH; enter zero (Ø). The sync waveform should then appear in total conformance to Figure 5 (page 40). There should be no horizontal rate pulses in the three line spacing preceding vertical sync. The horizontal sync pulses should shift to the left slightly, as there is to be no horizontal front porch for this format.

Note that now H front porch = 0 has been entered, it will remain in the system for all modes. This does, in effect, circumvent the inhibit built in the EDIT mode as discussed previously.

Enter Parameter 16, SYNC FORMAT; the display will read SYNC FORMAT CST5. The oscilloscope waveform will be similar to Figure 5 except that it will have zero horizontal front porch.

Enter Sync Format 4; the display will read SYNC FORMAT CST4. The oscilloscope waveform will be similar to Figure 5, except that it will have zero horizontal front porch.

Enter Sync Format 1; the display will show error code W1, indicating that an attempt has been made to develop the Broadcast format with zero front porch, an unallowable condition.

Enter Sync Format 2; the display will show error code W2 indicating that an attempt has been made to develop the Industrial sync format with zero front porch, an unallowable condition.

Select Parameter 5 and enter the correct value for H Front Porch (1.5 usec. for RATE 99 525/60). Enter Sync Format 4; the oscilloscope waveform should conform to Figure 5, Broadcast sync format. Select Parameter 17 (V FRNT POR), indicating a V front porch of six half lines containing six equalizing pulses. Enter V front porch of five half lines; the number of equalizing pulses should be reduced to five in the vertical front porch only. There will continue to be six serrations in the vertical sync interval and six equalizing pulses in the post equalizing interval.

NOTE: It is possible to transfer this "non-standard" format back into SYNC FORMAT 1 as long as the H front porch is something other than zero. In this way, the "standard" access codes could be used for a sync convention other than EIA standard formats. For example, in the EDIT mode, Custom 4, the vertical interval could be converted to CCIR format (five equalizing pulses, five serrations, five equalizing pulses) then transferred to SYNC FORMAT 1, leaving SYNC FORMAT 4 available for other waveform editing.

Enter Parameter 17 (V FRNT POR) at CST6, restoring the V front porch to the original configuration.

Re-enter the BROADCAST (selector code 1) sync format before proceeding to the next step.

10. Continue to observe the Sync output. Sync oscilloscope from the leading (-) of H Drive, sweeping scope at a convenient rate to show the H sync pulses.

11. The serrations will appear as a faint trace of positive pulse half way between the H sync pulses (usually 4.8 usec. wide for RATE 99). The trailing edge of this pulse is coincident with the leading edge of H sync. Enter Parameter No. 7, 2H SERR, and compare displayed value to oscilloscope measurement.

12. Observe the sync pulse, noting the width of front porch delay (usually 1.6 usec. for RATE 99). Enter Parameter No. 5, H FRNT POR, and compare displayed value to oscilloscope measurement.

    Check width of the horizontal sync pulse (usually 4.8 usec. wide for RATE 99). Enter Parameter No. 6, H SYNC, and compare displayed value to oscilloscope measurement.

    Equalizing pulses will appear as a faint trace inside the H sync pulse outline (usually 2.4 usec. wide for RATE 99). Enter Parameter No. 8, 2H EQUAL, and compare displayed value to oscilloscope measurement.

13. The TTL format Blanking and Sync pulse outputs are identical in pulse width and spacing to the Video format outputs, but are direct coupled, and have a nominal fixed output level of 0v. to +4v. unterminated. Connect each output to the oscilloscope to verify pulse shape and level with polarity (positive or negative pulse) as selected at the rear panel. Note that the TTL driver circuit does not produce as precise a waveform as the Video format; some crosstalk between channels is evident in the unloaded outputs. The outputs will appear much cleaner when loaded by a terminating resistor. Pulse polarity is selectable by the slide switch next to the connector on the rear panel.

    a. Sync the oscilloscope to the leading (-) edge of the H Drive output (Video format). Set oscilloscope sweep speed to view horizontal rate information.

    b. Connect the oscilloscope Channel 1 input to the Blanking output (Video format), and Channel 2 input to the Blanking output (TTL format). Use dual trace, alternate mode oscilloscope setting to compare the two waveforms, which should be of identical spacing and pulse width for both positive and negative polarity. Check the TTL format pulse for proper amplitude.

    c. Repeat Step b. for the Sync waveform.

    d. Repeat Step b. for the H Sync waveform. The H sync pulse is the same as the horizontal rate pulse in the composite Sync output, except that the pulse appears continuously, even through the vertical blanking interval. There are no equalizing pulses or serrations inserted into this output.

    e. Sync the oscilloscope to the leading edge (-) of V Drive (Video format), with the sweep speed to view vertical rate information. Repeat Steps b., c. and d. for the Blanking, Sync and V Sync waveforms (TTL format outputs), for vertical rate.

    f. Connect the oscilloscope Channel 1 input to the V Drive output (Video format), and Channel 2 input to the V Sync output (TTL format). The V sync pulse occurs three horizontal lines after the start of V drive, and is three lines wide (190 usec. for RATE 99). Compare the V sync pulse width to V drive for both polarities.

g. The V Trigger pulse is programmed for both position (phase as compared to the leading edge of V drive) and pulse width. There is no standard or common practice for settings, so pulse should be set as desired for the application.

Enter Parameter No. 14, V TRIG PH, and compare displayed value to oscilloscope measurement. Enter V Trigger position as desired. An entry of "0" will place the leading edge of V trigger coincident with the leading edge of V drive. An entry of "15" will delay the leading edge of V trigger for the time equal to 15 half lines (or 7.5 whole lines) past the leading edge of V drive (476.2 usec at RATE 99). Check that V trigger phase is equal to 0 lines for RATE 99.

Enter Parameter No. 15, V TRIG WID, and compare displayed value to oscilloscope measurement. Enter V Trigger width as desired. An entry of "0" is not considered a value operational setting. An entry of "23" will provide a pulse width equal to the time of 23 half lines (or 11.5 whole lines), 730.2 usec at RATE 99. Check that V trigger width is equal to 21 half lines for RATE 99.

h. The H Trigger output position and width may be programmed independently of the H drive waveform. Sync the oscilloscope from the leading edge (-) of H Drive, and view this waveform on Channel 1. View the H Trigger output on Channel 2, with oscilloscope sync set to view horizontal rate information. Enter "0" for Parameter No. 10, H TRIG PH; in this position the leading edge of the H Trigger output is coincident with the leading edge of H Drive. Enter some number, other than "0", for H TRIG PH. Observe position of the H trigger pulse to be as required for the application and compare displayed time to measured delay. Note that the range available allows the delay to extend to the end of the horizontal line, in effect placing the H trigger in advance to H drive leading edge, if so desired.

Measure the width of the H Trigger pulse. Enter Parameter No. 11, H TRIG WID, and compare displayed value to oscilloscope measurement.

14. The procedure just described will produce a 2:1 interlaced television rate, with pulses as detailed in Figure 23, page 66. A non-interlaced condition, sometimes referred to as 1:1 interlace or progressive scan, can be obtained by entering an even number of scan lines per two fields for Parameter No. 1, NO. LINES. To check this function:

a. Sync the oscilloscope from the leading edge (-) of V Drive, and set oscilloscope sweep rate to view an entire television vertical field. Use either the expanded sweep or delayed sweep to view the second vertical interval of the sync output, where a few lines can be observed before start of the V sync information. The number of scan lines per field may be checked by a frequency counter as described in Step 5, page 97.

b. Compare the Sync waveform in Figure 23, page 66, for an interlaced condition, which will develop 262.5 lines per field for RATE 99.

c. Enter 526 for Parameter No. 1, NO. LINES. Compare the sync waveform to Figure 23, page 66, for the non-interlaced condition, in which each field will be the same, not showing a half-line difference, developing 263 lines per field. Return entry to 525.

15. This completes performance verification of the programmable sync generator section.

Test Pattern Generator Section

There is no standard or even common prevailing practice which governs the test requirements or test pattern content for non-broadcast video systems. The calibration of pattern content is, therefore, somewhat arbitrary and may be set according to system specification requirements or prevailing common practice. In the absence of system standards to the contrary, it is suggested that:

a. Synchronizing pulses conform to the Vii Proportional Format.

b. Resolution pattern content be presented in the sequence of rep rate frequencies provided on the front panel. That is, the five bursts are presented in the order of 10, 15, 20, 25 and 30 mHz for whatever scan rate is in use.

c. The Window pattern provide a 25% duty cycle. Therefore, the white Window pattern would appear as a white rectangle in the center of a black background, the white center covering 25% of the total display area (25% white, 75% black). H Window parameters are calculated automatically in the H PATTERN STD mode (Parameter 20) or can be individually entered by H WIN START (Parameter 23) and H WIN STOP (Parameter 24) in the H PATTERN CUST mode. V Window parameters are programmed individually in the V WIN START (Parameter 27) and V WIN STOP (Parameter 28) modes at all times.

d. The Bars/Dots patterns be based on 17 vertical and 14 horizontal elements (i.e., 14 H Bars and 17 V Bars). V Bar parameters are calculated automatically in the H PATTERN STD mode (Parameter 20) or can be individually entered by V BAR POS (Parameter 21) and V BAR SPC (Parameter 22) in the H PATTERN CUST mode. H Bar parameters are programmed individually in the H BAR POS (Parameter 25) and H BAR SPC (Parameter 26) modes at all times.

e. The Gray Scale characteristic should be linear, composed of black, white and eight intermediate shades of gray.

There is no definitive standard on d.c. condition for video or synchronizing signals in television systems. The video output signal is direct coupled to avoid the slightest tilt in the video frame for some patterns. The blanking level (blacker-than-black) is at approximate ground (zero voltage) with the video portion positive going and sync portion negative going. Should this not be suitable for your application, please contact the factory.

Vii test pattern generators are calibrated upon the basis of active horizontal line time (total H line time minus the H blanking interval) and the active vertical field period (total scan lines per field minus the number of scan lines which occur in the V blanking interval).

Procedure

Generator performance is verified using an individual procedure for each test pattern, which is complete in itself except that the composite video output must be checked first to verify basic signal levels. For signals, observe the output composite video signal at the Composite Video Output connector on the rear panel. Refer to INTERNAL CONTROLS, page 33, if adjustments are necessary.

The television monitor should be underscanned (all raster edges visible) so that the entire pattern will be visible during pattern inspection. If the monitor is not underscanned, some bar, dot, gray scale, color bar, etc., elements may not be visible.

a. The synchronizing pulse inputs must have proper width and timing of H Drive, V Drive, Sync and Blanking pulses for proper operation of the pattern generator section. Pulse proportions can be programmed as desired (either proportional or custom) for the scan rate in use; sync generator section performance should be verified by the preceding procedure. It is convenient to have H Drive and V Drive available for oscilloscope sync purposes. Connect the test pattern generator for use as described in the CONNECTIONS section of this manual, as shown in Figure 1 (page 19).

b. The output connector must be terminated at the oscilloscope input using a UG-274/U BNC series coaxial cable tee and 75 ohm termination, as detailed in Figure 1 (page 19).

c. Connect oscilloscope Channel 1 input to the appropriate Composite Video Output connector at the rear panel using RG59B/U coaxial cable.

d. Set oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division, direct coupled, unless otherwise stated.

e. Controls are located on circuit cards inside the unit. Circuit cards and control locations are listed in the CIRCUIT CARD AND CONTROL LOCATIONS (page 29) and INTERNAL CONTROLS (page 33) sections.

f. Set oscilloscope sync on external, negative slope (-), a.c. coupled, unless otherwise noted.

g. Amplitude and impedance have been outlined in EIA Standards. Television systems universally are at 75 ohm cable impedance except for some specialized military systems which use 95, 91 or 51 ohms. A 75 ohm system is supplied unless otherwise specified as a modification. Video signal amplitudes may be at one of two common levels:

    1. An overall composite video signal of 1.0v., composed of a video maximum level of 0.714v. (including a blanking pedestal of 0.039v.) plus a sync level of 0.286v. on all three (Red, Green and Blue) video channels.

2. Video maximum level of 1.0v. (including a blanking pedestal of 0.055v.) plus sync of 0.4v., making an overall composite video signal of 1.4v. pk-pk. This is accomplished by removing R38 from each of the TTL VIDEO circuit cards (Positions 3C, 4C and 5C). A slight trimming adjustment of video and sync levels may be required to obtain exactly 1.4v. composite video.

This instrument has been configured at the factory (unless otherwise specified) for a maximum 1.0v. composite video signal (0.714v. video + 0.286v. sync) on all three (Red, Green and Blue) video channels.

The test pattern section has the normal composite video output at "standard" television system levels and impedance plus a TTL level output of nominal +4.0v. ±0.7v. (unterminated) pk-pk voltage at a nominal 75 ohm output impedance. The TTL output contains only video information of digital data; it does not offer a blanking pedestal or sync. The TTL level output is intended to be used only for short cable runs, not over long lengths of coaxial cable.

h. This procedure is written on the basis of the 525/60 scan rate as programmed. If this is not the case, timing will vary. Examples for other scan rates are shown in Tables I, II and III.

i. Test patterns may be viewed on either an RGB color or monochrome television monitor. If using a color monitor, all three outputs should be connected to develop a white pattern on a black background. The monitor may be synchronized internally from the G channel composite signal, or may be synchronized externally using pulse outputs from the test pattern generator.

For most patterns, the output signal is identical on the Red (R), Green (G) and Blue (B) channels. Generally the signal can be monitored on any one channel as desired, except for the Color Bars and Combination functions. The procedure assumes that identical signal format (composite or non-composite) is desired on all channels. However, some systems may require a composite signal on the G channel, and a non-composite signal on the R and B channels; this is easily obtained by adjusting the Sync Level control (R41) to zero on the red and blue channel TTL VIDEO circuit cards (Positions 3C and 5C only). Control location is at the left side on the TTL VIDEO R and B circuit cards.

Video Signal Verification

The level of the video, blanking pedestal and sync portions of the composite video signal output must be verified before inspecting pattern content. Black level, risetime and output impedance must be checked as well. These tests can be conducted even though pattern proportions may not be adjusted to the exact value required.

In a generator with the separate RGB (red, green and blue) outputs, each output must be calibrated individually. However, the green channel is the primary one; the red and blue outputs should be adjusted to conform to the green output levels.

This test sequence involves the following circuit cards:

2155 TTL VIDEO . . . . . Positions 3C, 4C, 5C
4010 VIDEO CONTROL . . . Position 3B

Each channel of the triple RGB outputs must be set up individually. The G (green) channel is primary, and does not contain a trimmer video level control. The R (red) and B (blue) channel outputs do use a trimmer video level control (R2, VIDEO GAIN located on the TTL VIDEO R and B circuit cards) to allow amplitude of these channels to be matched to the green channel level. This test procedure is to calibrate the green channel first for basic levels, then trim the red and blue channels to match.

1. Connect the equipment for test as shown in Figure 1 (page 19). Set the oscilloscope sweep speed to view horizontal rate information.

2. Set oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

3. Connect the oscilloscope external sync to the H Drive source. Sync the oscilloscope externally, negative slope.

4. Connect a coax cable to the Composite Video G output connector and oscilloscope Channel 1 input, terminated at the oscilloscope input.

5.* A Black Level control (R8) is located on the VIDEO CONTROL circuit card (Position 3B) for precise setting of the Gray Scale waveform black level to ground potential (0v.). This control must be adjusted for optimum signal condition, with black level at ground (0v.) potential. A test point is provided on the circuit card for assistance in this test.

   Select GRAY SCALE at the front panel. Using a high impedance oscilloscope probe, observe the signal at the test point at the right side on the VIDEO CONTROL (Position 3B) circuit card. The black level (first "step" and through blanking) should be at ground potential, 0v.

Adjust the Black Level control (located at the center position) on the VIDEO CONTROL circuit card (Position 3B) for this condition, if required. Compare oscilloscope display to Figure 14a (page 50). Adjustment made for the G (green) channel only and is not changed for the R (red) or B (blue) channels.

6. Select the V STRIPE function at the control panel. Compare oscilloscope display to Figure 15a (page 51) to identify and check level of the video, blanking and sync portions of the signal.

7. Black level of the V Stripe must be checked to match the black level of the Gray Scale. This test must be made individually for each one of the triple RGB outputs.

   The optimum setting is a compromise at best, and misadjustment can cause signal distortion. Common problems to be watched for include:

   a. Black Level Clipper too low . . . pedestal will appear higher on Bars, Dots, Window and related signals as compared to the Gray Scale signal, and the pedestal level will appear to vary as the Blanking Level control is turned up and down.

   b. Black Level Clipper too high . . . bottom of Gray Scale will "push down" into the sync portion of the signal, and it may be necessary to adjust the Black Level control on the TTL VIDEO circuit cards before the Bars, Dots, Window and related signals will appear from black level. Extreme misadjustment may cause lower steps of the Gray Scale to be clipped or compressed. Check the Video G output, connected to oscilloscope Channel 1 and terminated, for either of these conditions.

   Select the V STRIPE pattern. While observing the waveform at horizontal rate, align black level to the center of the graticule by use of the oscilloscope horizontal and vertical Position control. Make sure oscilloscope input is direct (d.c.) coupled for this check and do not readjust waveform position on the oscilloscope display.

   Select GRAY SCALE at the control panel. If Gray Scale black level shifts, black level adjustment is required.

8.* If adjustment is necessary, adjust the sync level to 0v. (maximum counterclockwise position) by use of the Sync Level control (R41) located at the left side on the TTL VIDEO G (Position 4C) circuit card.

   Adjust the blanking level to 0v. (maximum counterclockwise position) by use of the Blanking Level control (R47) at second position from left side on the TTL VIDEO G (Position 4C) circuit card. The waveform visible is the video portion of the signal.

   Select GRAY SCALE. Adjust the Black Level control (R8, located at the fifth position from left on the TTL VIDEO G circuit card in Position 4C) to the point where black levels are the same as observed while switching back and forth between the GRAY SCALE and V STRIPE functions.

9. Several signal level standards exist in the video industry, as described on page 104 (Step g.). This instrument normally is calibrated to provide a 1.0v. composite video signal (0.714v. video plus 0.286v. sync). If a 1.4v. video signal (1.0v. video plus .4v. sync) is desired, remove resistor R38 from each of the TTL VIDEO circuit cards in Positions 3C, 4C and 5C. Select the V STRIPE pattern for signal level calibration.

10.* Adjust the Blanking Level control (R47, located at second position from left side on the TTL VIDEO G circuit card in Position 4C) to obtain desired blanking pedestal level, nominally 0.039v.

11.* Adjust the Sync Level control (R41, located at the left side on the TTL VIDEO G circuit card in Position 4C) to set amplitude of the sync portion of the signal at 0.286v. or other desired amplitude.

12.* Adjust the White Level control (R16) at the right side on the VIDEO CONTROL (Position 3B) circuit card to give 0.714v. or other desired limit of video portion of the composite video signal including 0.039v. blanking level. The composite video signal should then be 1.0v. peak-to-peak (0.714v. video with 0.039v. blanking pedestal + 0.286v. sync). This adjustment is made for the G (Green) channel only.

13.* If the levels are to be calibrated for less than maximum values, reduce the amplitudes obtained in Steps 10 through 12 as required. Check that the blanking level is at 0v. d.c. position (ground).

Adjust the Comp Offset control (R50) located at third position from left side on the TTL VIDEO G circuit card in Position 4C to set the blanking interval at 0v. (ground) d.c. level. This control will cause the entire composite video signal to shift vertically on the oscilloscope screen without affecting signal levels.

14. To check source impedance, remove the termination at the coax tee at oscilloscope Channel 1 input. The signal level should double that set in Steps 10 through 13. There is no adjustment for impedance; a discrepancy of more than $\pm$10% would indicate that repair is required. Replace the termination.

15. Connect the coaxial cable to the TTL Video G output connector on the rear panel and oscilloscope Channel 1 input. Set oscilloscope sensitivity at 1.0v. per division. Do <u>not</u> terminate the coax cable.

16. Select the V STRIPE function at the control panel. Compare oscilloscope display to Figure 15a to identify and check level of the TTL video to be 4.0v. $\pm$0.7v. (unterminated). Blanking and sync portions of the signal will not be present. The maximum level of TTL video is established by composite signal adjustments of Step 13, and is not set separately.

17. Install a 75 ohm termination at the coax cable at the oscilloscope Channel 1 input. The TTL video signal level should drop to half of the level observed in Step 16.

18. This completes calibration of the Green channel.

19. The procedure detailed below should be completed for the Red (R) channel.

20. Connect the oscilloscope Channel 1 input to the Composite Video R output connector, terminated at the oscilloscope input. Set Channel 1 sensitivity at 0.5v. per division.

21.* Select the GRAY SCALE function at the front panel. Observe the black step (first on the left to the right of the horizontal blanking interval) at the center of the oscilloscope graticule by use of the oscilloscope horizontal and vertical Position control. Black level of the Gray Scale was set previously while in the G (Green) channel (Step 5); DO NOT readjust controls on the VIDEO CONTROL circuit card for the Red or Blue channels.

22.* If Gray Scale black level shifts, black level adjustment is required. Adjust the Sync Level control (R41) to 0v. (maximum counterclockwise position) by use of the control located at the left side on the TTL VIDEO R (Position 3C) circuit card.

Adjust the Blanking Level control (R47) to 0v. (maximum counterclockwise position) by use of the control located at second position from left side on the TTL VIDEO R (Position 3C) circuit card.

The only waveform visible would be the video portion of the signal.

23. Select V STRIPE at the front panel and align black level to the center of the oscilloscope graticule by use of the horizontal and vertical Position control.

Select GRAY SCALE. Adjust the Black Level control (R8, located at the fifth position from left on the TTL VIDEO R circuit card in Position 3C) to the point where black levels are the same as observed while switching back and forth between the GRAY SCALE and V STRIPE functions.

24.* Adjust the Blanking Level control (R47, located at the second position from left on the TTL VIDEO R circuit card in Position 3C) to obtain desired blanking pedestal level, nominally 0.039v.

25.* Adjust the Sync Level control (R41, located at the left side on the TTL VIDEO R circuit card in Position 3C) to set amplitude of the sync portion of the signal at 0.286v. or other desired amplitude.

26.* Adjust the Video Gain control (R2, located at the fourth position from left side on the TTL VIDEO R circuit card in Position 3C) to obtain 1.0v. peak-to-peak video amplitude.

27. If values are to be calibrated for less than maximum values, reduce the amplitudes obtained in Steps 23 through 25 as required. Check that the blanking interval is at 0v. d.c. position (ground).

    Adjust the Comp Offset control (R50, located at third position from left side on the TTL VIDEO R circuit card in Position 3C) to set the blanking interval at 0v. (ground) d.c. level. This control will cause the entire composite video signal to shift vertically on the oscilloscope screen without affecting signal levels.

28. To check source impedance, remove the termination at the coax tee at oscilloscope Channel 1 input. The signal level should double those set in Steps 24 through 26. There is no adjustment for impedance; a discrepancy of more than ±10% would indicate that repair is required. Replace the termination.

29. Connect the coaxial cable to the TTL Video R output connector on the rear panel and oscilloscope Channel 1 input. Set oscilloscope sensitivity at 1.0v. per division. Do not terminate the coax cable.

30. Select the V STRIPE function at the control panel. Compare oscilloscope display to Figure 15a (page 51) to identify and check level of TTL video to be +4.0v. ±0.7v. (unterminated). Blanking and sync portions of the signal will not be present.

    The maximum level of TTL video is established by composite signal adjustments of Step 27, and is not set separately.

31. Install a 75 ohm termination at the coax cable at the oscilloscope Channel 1 input. The TTL video signal level should drop from +4.0v. peak to a nominal 2.0v. peak.

32. This completes calibration of the Red channel. Repeat Steps 20 through 31 for the B (Blue) channel using appropriate controls on the TTL VIDEO B circuit card in Position 5C. Proceed to the following general adjustments.

33.* Select the Non-composite output signal mode by adjusting the Sync Level control (R41, located at the left side on each of the TTL VIDEO circuit cards) to zero. The sync portion of the composite video should disappear.

34.* Return the Composite signal mode by readjusting the Sync Level control (R41) on each of the TTL VIDEO circuit cards to 0.286v.

35. This completes Video Signal Verification.

36. Connect the Video Output to the monitor input as shown in Figure 1 (page 19). A monochrome monitor may be used to view the output channels individually. If a color monitor is available, connect the red, green and blue cables to the appropriate monitor input connectors. A V Stripe pattern should be obtained with no visible hum or interference.

37. This completes Video Signal Verification for all channels.

38. When all parameters have been programmed and signal level adjustments have been made, an access code must be assigned designating a specific scan rate to a given memory location. Blank RASTER SUMMARY forms are found in the RasterMaster Log and should be filled out when programming parameters.

    The Model 2501 contains a permanent "default rate", Access Code 99, which is stored in permanent inaccessible memory. No other scan rate can be stored in this memory location.

    The generator has been tested at the factory with several scan rates as itemized in the RasterMaster Log (Access Codes 10, 11, 12 and 13). If other scan rates are stored in these memory locations, corresponding RASTER SUMMARY forms should be discarded. Note that this instrument provides for up to 69 separate raster structures.

    At the RASTER NUM prompt, enter access code to be assigned to the scan rate just programmed. Press ENTER.

FLAT FIELD

Circuit cards involved in the Flat Field function include:

4010	VIDEO CONTROL	Position 3B
4000	GRAY SCALE	Position 4B

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set oscilloscope sweep rate to view vertical information.

3. Set oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect the oscilloscope external sync input to the V Drive source. Synchronize the oscilloscope externally, negative slope.

5. Select the FLAT FIELD function at the front panel.

6. Compare oscilloscope display to Figure 7b (page 42). This instrument is designed to provide 50% gray level in the Flat Field function.

   Some applications require the Flat Field level to be at 100% white. This can be obtained by removing the specified jumper from the GRAY SCALE circuit card. There will not be any adjustment of Flat Field in this mode. Refer to drawing L-4000 (GRAY SCALE) at the rear of this manual.

7.* Flat Field normally is adjusted to be 50% gray level to preserve 50% Average Picture Level (APL) in the output pattern. The Flat Field Level control (R18) located at second from left side on the GRAY SCALE (Position 4B) circuit card is used to adjust Flat Field level. Nominal control range is from .26v. to .54v.; gray level should be adjusted to 0.357v. for video with 0.714v. white level.

8. Set oscilloscope sweep to view horizontal information.

9. Connect the oscilloscope external sync output to the H Drive source. Synchronize the oscilloscope externally, negative slope.

10. Compare oscilloscope display to Figure 7a (page 42).

11. The composite R (red) and B (blue) channels contain the same video pattern signal as the G (green) channel. Repeat Step #10 for the R and B channels using the appropriate composite video output connectors on the rear panel. Check that the Composite Video R and Video B Outputs are identical to the Composite Video G Output.

12. TTL video R (red) and B (blue) channels contain the same video pattern signal as the TTL video G (green) channel. Check that the TTL Video R and B Outputs are identical to the TTL Video G Output.

13. Observe the composite video portion of the signal; video, blanking and sync should remain at the levels set in Video Signal Verification (page 106).

14. Observe the TTL video portion of the signal. The video portion should remain at the levels observed in Video Signal Verification (page 106). Blanking and sync portions of the TTL signal will not be present.

15. Connect the Video Output to the monitor to display the Flat Field pattern which should appear as a flat white pattern with no visible hum or interference.

16. Performance verification of the Flat Field function is now complete.

BARS and DOTS

The Bars and Dots patterns are related, derived from common horizontal and vertical pattern elements. Therefore calibration is considered for both functions. Circuit cards involved include CLOCKED BAR/DOT (4003) in Position 8B.

The user has a choice of two modes for pattern development of the Bars and Dots functions. Selection of either the STD or CUST mode is selected during programming. The STD mode automatically calculates position of vertical bar elements. The CUST mode allows the user to program position of the first vertical bar from the left side of the display and also spacing between vertical bars.

Vertical Bar Elements

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set oscilloscope sweep to view horizontal information.

3. Set the oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect the oscilloscope external sync connector to the H Drive source. Synchronize the oscilloscope externally, negative slope.

5. Select the BARS function at the front panel.

6. Compare oscilloscope display to Figure 10 (page 46). Vertical bar elements are shown as programmed by H PATTERN (Parameter 20) STD mode. Select the standard mode by entering one (1) at the H PATTERN prompt (Parameter 20).

   The number of elements generated in the horizontal t.v. field in the standard mode is clocked from 20H and may not be varied in position or spacing. There should be 17 elements across the active horizontal line as shown in Figure 10 (page 46).

   If standard proportion is not appropriate, spacing and position of vertical bar elements can be developed to suit any application using the custom mode instead. Select the custom mode by entering zero (Ø) at the H PATTERN prompt (Parameter 20). Pattern proportions were initially entered when scan rates were programmed. Parameter 21 (V BAR POS) programs timing desired for position of the first V bar element. Parameter 22 (V BAR SPC) programs spacing between elements in the vertical plane. Refer to the TO EXAMINE OR EDIT (MODIFY) PARAMETERS IN A SCAN RATE PREVIOUSLY STORED flow chart (page 87) for proper editing procedure, if required.

7. Set oscilloscope delayed sweep to 0.1 usec. per division and adjust the sweep delay time to show one bar element. The DOT WIDTH potentiometer control on the front panel is used to adjust the size of vertical bar elements; this control also adjusts width of the elements in the Dots pattern. Pulse width should vary from approximately 50 nsec. to 250 nsec. The pulse may appear to "drop out" at the extreme counter-clockwise control setting, but reappear as the control is turned clockwise. Return oscilloscope to A sweep (undelayed). Dot width usually is set to 0.10 usec. ($\pm$0.05 usec.) or other desired width.

Horizontal Bar Elements

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set oscilloscope sweep to view vertical information.

3. Set the oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect the oscilloscope external sync connector to the V Drive source. Synchronize the oscilloscope externally, negative slope.

5. Select the BARS function at the front panel.

6. Compare oscilloscope display to Figure 11 (page 47).

7. Nominal setting is 14 H bar elements in the television field.

8. Position and spacing of horizontal bar elements were entered initially when scan rates were programmed at the H BAR POS (Parameter 25) and H BAR SPC (Parameter 26) prompts. The STD mode does not apply to horizontal bar elements.

   Refer to the TO EXAMINE OR EDIT (MODIFY) PARAMETERS IN A SCAN RATE PREVIOUSLY STORED flow chart (page 87) for proper editing procedure, if it is necessary to edit position and spacing parameters.

Dots

Position and proportion of the Dots pattern elements are determined by the Bars pattern, for dots are generated at the intersection of the H and V elements in the Bars pattern. Dot size is adjustable as outlined under Vertical Bar Element calibration.

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set the oscilloscope sweep rate to view vertical information.

3. Set oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect oscilloscope external sync connector to the V Drive source. Synchronize the oscilloscope externally, negative slope.

5. Select the DOTS pattern at the front panel.

6. Compare oscilloscope display to Figure 13 (page 49).

7. Location of the vertical dot elements is the same as for vertical bar elements. Expand the oscilloscope sweep to check that spacing and position continue to be the same as observed for vertical bar elements. Return to normal sweep.

8. Location of the horizontal dot elements is the same as for horizontal bar elements; check that spacing and position continue to be the same.

BARS and DOTS

1. The procedure just outlined involves the composite G (green) channel only. The R (red) and B (blue) channels contain the same video pattern signal. Check that the Composite Video R and Video B outputs are identical to the Composite Video G output.

2. TTL video R (red) and B (blue) channels contain the same video pattern signal as the TTL video G (green) channel. Check that the TTL Video R and B Outputs are identical to the TTL Video G Output.

3. Observe the composite video portion of the signals; video, blanking and sync should remain at the levels set in Video Signal Verification (page 106).

4. Observe the TTL video portion of the signals. The video portion should remain at the levels observed in Video Signal Verification (page 106). Blanking and sync portions of the TTL signal will not be present.

5. Connect the Video Output to the monitor to display the Bars and Dots patterns individually. Check that horizontal and vertical bar elements are straight, and that the Bars pattern is a combination of horizontal and vertical pattern elements. Dot elements should occur at the intersection of horizontal and vertical bar elements.

6. Performance verification of the Bars and Dots functions is now complete.

GRAY SCALE

The Gray Scale signal is composed of ten levels of brightness, including black and white. Therefore the traditional "ten step" scale actually is composed of nine risers, and eight shades of gray between the extremes. Gray Scale position is automatically determined by the computer and is not adjustable. Existing standards and common practice call for a linear Gray Scale test signal (one with all steps of equal amplitude). Circuit cards involved include:

4010	VIDEO CONTROL	Position 3B
4000	GRAY SCALE	Position 4B
4007	GRAY SCALE SELECT	Position 5B

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set the oscilloscope sweep speed to view horizontal information.

3. Set oscilloscope Channel 1 input amplitude sensitivity at 0.2v. per division. Oscilloscope sweep rate should show the entire horizontal line when using horizontal related sync and observations.

4. Connect oscilloscope external sync to the H Drive source. Synchronize the oscilloscope externally, negative slope.

5. Set Function Selector switch at GRAY SCALE.

6. Compare oscilloscope display to Figure 14a (page 50).

7. The following adjustment procedure assumes that the Black Level (R8) and White Level (R16) controls located on the VIDEO CONTROL circuit card in Position 3B are properly adjusted, as set forth in Signal Level Adjustments (page 106).

8. Using the Uncal control at the oscilloscope input, reduce pattern amplitude so that the first step of Gray Scale (not including the blanking pedestal) is positioned at the center graticule on the oscilloscope grid. The tenth level (white)should then be positioned at the 0.9v. grid line.

9. Check that there is a linear staircase presentation with steps of uniform level; one level will be on each minor graticule division on the oscilloscope grid. If there is any deviation from Figure 14a (page 50), calibration should be performed as outlined below. If other than a linear stairstep presentation is desired, a revised procedure should be followed which will obtain that presentation.

10.* Potentiometers on the GRAY SCALE circuit card (Position 4B) should be adjusted in proper sequence from white to black while observing the signal on an oscilloscope. Using the control located at fourth from the left side of the circuit card, adjust the level of the first step down from white to one minor division (0.1v.) below white level. Using the next control located at fifth from the left side of the GRAY SCALE circuit card, adjust the second step to one minor division (0.1v.) from the previous step. Moving to the next control, adjust the third step, fourth step, etc., using the appropriate controls on the GRAY SCALE card until all eight steps between black and white have been adjusted to 0.1v. each. The horizontal and vertical positions of the oscilloscope display may be shifted to place the step under adjustment at the center graticule lines for convenience in adjustment of the Gray Scale levels. There should be a Gray Scale step at each minor division on the graticule when adjustment is proper. Return oscilloscope to initial settings.

11. The length of scanning line in which the Gray Scale is presented is clocked and not adjustable. A proper Gray Scale shows one increment of white level signal at the right end of the t.v. line equal to other Gray Scale step widths. A complete presentation should show black level, eight shades of intermediate Gray Scale level as adjusted, and the final white level plateau.

12. Set oscilloscope sweep rate to view vertical information.

13. Connect the oscilloscope external sync connector to the V Drive source. Synchronize the oscilloscope externally, negative slope.

14. Compare oscilloscope display to Figure 14b (page 50).

15. The procedure just outlined involves the composite G (green) channel only. The R (red) and B (blue) channels contain the same video pattern signal. Check that the Composite Video R and Video B Outputs are identical to the Composite Video G Output.

16. TTL video R (red) and B (blue) channels contain the same video pattern signal as the TTL video G (green) channel. Check that the TTL Video R and B Outputs are identical to the TTL Video G Output.

17. Observe the composite video portion of the signal; video, blanking and sync should remain at the levels set in Video Signal Verification (page 106).

18. Observe the TTL video portion of the signal. The video portion should remain at the levels observed in Video Signal Verification (page 106). Blanking and sync portions of the TTL signal will not be present.

19. Connect the Video Output to the monitor to display the Gray Scale pattern. A clear, well defined Gray Scale with all lines straight should be obtained.

20. Performance verification of the Gray Scale function is now complete.

V STRIPE and WINDOW

The V Stripe and Window patterns are related, derived from common vertical elements. Therefore, programming of vertical pattern elements is considered for these patterns as a group. Circuit cards involved include PATTERN LOGIC (4006) in Position 9B.

The Window is a white rectangle surrounded by a uniform black background over the remainder of the raster. This pattern provides a thorough evaluation of low frequency response, as evidenced by tilt in the vertical rate waveform. The sharp transition from black to white and white to black at the edges of the Window in the horizontal dimension provides a convenient tool for analysis of transient response also.

V Stripe is a strip the entire height of the display whose width is the same as the Window rectangle. This pattern usually provides an approximate 50% duty cycle (APL), thus preventing the development of distortion which may be present during the lower APL of the Window signal. The center area of the V Stripe waveform oscilloscope trace will be brighter than the vertical Window waveform trace, since elements are developed in every line of the active raster rather than just a few.

V Stripe

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set the oscilloscope sweep speed to view horizontal information.

3. Set oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect oscilloscope external sync to the H Drive source. Synchronize the oscilloscope externally, negative slope.

5. Set Function Selector switch to V STRIPE.

6. Compare oscilloscope display to Figure 15a (page 51). Standard V Stripe proportion of the white area is 0.50h (50% of the active portion of the horizontal line), automatically calculated in the H PATTERN (Parameter 20) STD mode as shown in Figure 15a. Select the standard mode by entering one (1) at the H PATTERN prompt (Parameter 20).

   The V Stripe waveform trace of the center area is brighter than the trace will appear in the Window waveform since elements are developed in every line of the active raster.

   If standard proportion is not appropriate, width and position of the V Stripe function can be developed to suit any application using the custom mode instead. Select the custom mode by entering zero (Ø) at

the H PATTERN (Parameter 20) prompt. Pattern proportions were initially entered when scan rates were programmed. Width and position of the V Stripe function can be programmed with the H WIN START (Parameter 23) and H WIN STOP (Parameter 24) prompts. These parameters should provide virtually any H position and H width desired for the V Stripe pattern. Refer to the TO EXAMINE OR EDIT (MODIFY) PARAMETERS IN A SCAN RATE PREVIOUSLY STORED flow chart (page 87) for proper editing procedure, if required.

Window - Horizontal Elements

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set oscilloscope sweep speed to view vertical information.

3. Set oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect oscilloscope external sync to the V Drive source. Synchronize the oscilloscope externally, negative slope.

5. Select the WINDOW function at the front panel.

6. Compare oscilloscope display to Figure 15b (page 51). Standard Window proportion of the white area is 0.50h (50% of the active portion of the horizontal line), automatically calculated in the H PATTERN (Parameter 20) STD mode as shown in Figure 15b. Select the standard mode by entering one (1) at the H PATTERN prompt (Parameter 20).

   If standard proportion is not appropriate, width and position of the Window function can be developed to suit any application using the custom mode instead. Select the custom mode by entering zero (Ø) at the H PATTERN (Parameter 20) prompt. Pattern proportions were initially entered when scan rates were programmed. Width and position of the Window function can be programmed with the H WIN START (Parameter 23) and H WIN STOP (Parameter 24) prompts. These parameters should provide virtually any H position and H width desired for the Window pattern. Horizontal width of the Window is always the same as that of the V Stripe. Refer to the TO EXAMINE OR EDIT (MODIFY) PARAMETERS IN A SCAN RATE PREVIOUSLY STORED flow chart (page 87) for proper editing procedure, if required.

Window - Vertical Elements

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set oscilloscope sweep speed to view horizontal information.

3. Set the oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect the oscilloscope external sync to the H Drive source. Synchronize the oscilloscope externally, negative slope.

5. Select the WINDOW function at the front panel.

6. Compare oscilloscope display to Figure 15a (page 51).

7. Height of the Window rectangle was programmed (usually to provide a window height of 0.50v, 50% of the vertical portion of the vertical field, as shown in Figure 15a) initially when scan rates were programmed at the V WIN START (Parameter 27) and V WIN STOP (Parameter 28) prompts. The STD mode does not apply when programming vertical window parameters as in the case with programming horizontal window placement.

   Refer to the TO EXAMINE OR EDIT (MODIFY) PARAMETERS IN A SCAN RATE PREVIOUSLY STORED flow chart (page 87) for proper editing procedure, if it is necessary to edit vertical window parameters.

V STRIPE and WINDOW

1. The procedure just outlined involves the composite G (green) channel only. The composite R (red) and B (blue) channels contain the same video pattern signal. Check that the Composite Video R and Video B Outputs are identical to the Composite Video G Output.

2. TTL video R (red) and B (blue) channels contain the same video pattern signal as the TTL video G (green) channel. Check that the TTL Video R and B Outputs are identical to the TTL Video G Output.

3. Observe the composite video portion of the signals; video, blanking and sync should remain at the levels set in Video Signal Verification (page 106).

4. Observe the TTL video portion of the signals. The video portion should remain at the levels observed in Video Signal Verification (page 106). Blanking and sync portions of the TTL signal will not be present.

5. Connect the Video Output to the monitor to display the V Stripe and Window patterns individually. A white window on black background with straight edges and no distortion covering 25% of the raster area should be obtained as programmed for the Window function. The V Stripe pattern should appear as a white stripe at the center of the raster covering 50% of the width of the raster.

6. Performance verification of the V Stripe and Window functions is now complete.

RESOLUTION

This function includes several operating conditions and modes, each of which must be calibrated independently. The most common basis for calibration in signal repetition rate is resolution in t.v. lines, as detailed in Table II, CCTV Resolution Timing (page 54). Calibration can be based on other standards, such as burst frequency, or on other customer specified conditions. Control panel markings are 1 through 5 for the Resolution function, therefore allowing various calibration basis. This function involves the following circuit cards:

4000	GRAY SCALE	Position 4B
4002	RESOLUTION CONTROL	Position 7B
4013	RESOLUTION	Position 7C

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set oscilloscope sweep rate to view horizontal information.

3. Set the oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect the oscilloscope external sync connector to the H Drive source. Synchronize the oscilloscope externally, negative slope.

5. Set the Function Selector switch at RESOLUTION and Resolution Selector on REFERENCE.

6. The display should appear similar to Figure 17 (page 55) showing 17 cycles of black/white pattern across the horizontal line. The waveform should be square, without ringing or overshoot. This pattern is computed; the number of bars is not adjustable.

   CAUTION: Measurement technique regarding ringing and overshoot is critical on the fast rise Resolution signal. The case of the instrument under test should be firmly grounded to the cases of all other instruments being used. Attention should be paid to coaxial cable grounds to view the optimum output signal from the instrument. The oscilloscope risetime capability must be verified before the output of the instrument may be fully evaluated.

7. Select RESOLUTION REP RATE 1 at the front panel. Compare oscilloscope display to Figure 16a (page 53). Resolution bursts may be calibrated to various repetition rates as required by a particular application. Unless otherwise specified, the bursts will be adjusted as shown in Table II (page 54). Burst 1 usually is at 10 mHz rep rate. There should be bursts, cycles of black/white pattern in location of the white segments of the REFERENCE pattern. The bursts are separated by a 50% gray level video signal. The selected rep rate is presented over the entire display.

8. Set oscilloscope on delayed sweep (0.1 usec. per division sweep time), placing the delayed portion of the sweep on the horizontal line to observe the detail of the Resolution waveform. The signal should have approximately 10 nsec. rise and fall times with a minimum of overshoot and/or ringing. Individual black/white cycles should have 0.10 usec. (100 nsec.) duration.

9.* Select each resolution rate in turn, adjusting the appropriate Resolution Rep Rate control on the RESOLUTION circuit card (Position 7C) to obtain the resolution density set forth in Table II (page 54). This adjustment should be made while observing bar width on a precisely calibrated oscilloscope.

Control locations on the RESOLUTION (Position 7C) circuit card are as follows:

Rep Rate 1	Right side
Rep Rate 2	Second from right side
Rep Rate 3	Third from right side
Rep Rate 4	Fourth from right side
Rep Rate 5	Fifth from right side

10.* Using the Resolution Balance control at the left side on the RESOLUTION circuit card in Position 7C, adjust the burst cycle to be symmetrical (the same width of alternate black and white resolution pattern elements) for Rep Rate 3.

11. The space between bursts should be at 50% gray level (halfway between black and white amplitudes).

12.* Adjust the average picture level as desired using the Burst APL control located at third from the left side on the GRAY SCALE (Position 4B) circuit card. This is normally adjusted to provide a 50% gray level between each resolution burst.

13. Set oscilloscope sweep rate to view vertical information.

14. Connect the oscilloscope external sync connector to the V Drive source. Synchronize the oscilloscope externally, negative slope.

15. Compare oscilloscope display to Figure 16b (page 53).

16. The procedure just outlined involves the composite G (green) channel only. The R (red) and B (blue) channels contain the same video pattern signal. Check that the Composite Video R and Video B Outputs are identical to the Composite Video G Output.

17. TTL video R (red) and B (blue) channels contain the same video pattern signal as the TTL video G (green) channel. Check that the TTL Video R and B Outputs are identical to the TTL Video G Output.

18. Observe the composite video portion of the signal; video, blanking and sync should remain at the levels set in Video Signal Verification (page 106).

19. Observe the TTL video portion of the signal. The video portion should remain at the levels observed in Video Signal Verification (page 106). Blanking and sync portions of the TTL signal will not be present.

20. Connect the Video Output to the monitor to display the Resolution pattern. Check that all bursts are stable and in straight vertical columns. A clear, well defined Resolution pattern should be obtained at each control setting, depending on the quality of the display device.

21. Performance verification of the Resolution function is now complete.

COLOR BARS

The Color Bars function develops an eight step pattern of traditional format, including a white reference bar near the left side of the display (start of the horizontal line) and a black bar near the right side of the display (end of line). The pattern includes a narrow black strip at the left side and white strip at the right side. These strips serve as edge indicators, and prevent the pattern from being obscured by display overscan. Pattern proportions of the Color Bars function are computed, and are not adjustable. Circuit cards involved include:

2155	TTL VIDEO R	Position 3C
2155	TTL VIDEO G	Position 4C
2155	TTL VIDEO B	Position 5C
4008	CLOCKED COLOR BAR	Position 6C

The output video signals have been adjusted to provide a composite signal on the R (red), G (green) and B (blue) channels. Repeat the Signal Level Adjustments procedure (Step #33, page 110) if format is not correct as required for the particular system in use.

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set oscilloscope sweep rate to view horizontal information.

3. Set the oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect the oscilloscope external sync to the H Drive source. Synchronize the oscilloscope externally, negative slope.

5. Select the COLOR BARS function at the front panel.

6. Compare oscilloscope display to Figure 18c (page 57).

7. Check that one complete cycle of color bars, green component, is presented in the active horizontal scanning line length as shown in Figure 18c (page 57). The Color Bars pattern is clocked, therefore, not adjustable.

8. Connect the oscilloscope input to the Video R Output connector at the rear panel. Two complete cycles of color bars should be presented in the active horizontal scanning line length, per Figure 18b (page 57).

9. Connect the oscilloscope input to the Video B Output connector at the rear panel. Four complete cycles of color bars should be presented in the active horizontal scanning line length, per Figure 18a (page 57).

10. TTL video R (red), G (green) and B (blue) channels are identical to the composite video R, G and B channels.

11. Observe the composite video portion of the signal; video, blanking and sync should remain at the levels set in Video Signal Verification (page 106).

12. Observe the TTL video portion of the signal. The video portion should remain at the levels observed in Video Signal Verification (page 106). Blanking and sync portions of the TTL signal will not be present.

13. Connect the Video Output to the monitor. If a color monitor is used, vertical bars of various colors should be obtained for the Color Bars function, as identified by Figure 18 (page 57). If a monochrome monitor is used, look at each segment component individually in which there will be black and white bar patterns of different repetition rates, showing one cycle for green, two cycles for red, and four cycles for blue.

14. Performance verification of the Color Bars function is now complete.

VIDEO

The Video test pattern is a composite of Resolution, Black Reference and Gray Scale information. The Resolution Multiburst segment, composed of five bursts, is developed in the left half of the television line, the Black Reference segment at the center, and the Gray Scale is presented in the right half of the television line. These individual functions should have been verified prior to selection of the Video test pattern. The white level before and after the Black Reference segments serves as a maximum contrast for both the Resolution and Gray Scale patterns. The Video function is developed by the following circuit cards:

4000	GRAY SCALE	Position 4B
4007	GRAY SCALE SELECT	Position 5B
4001	VIDEO CLOCK	Position 6B
4002	RESOLUTION CONTROL	Position 7B
4006	PATTERN LOGIC	Position 9B
4008	CLOCKED COLOR BAR	Position 6C
4013	RESOLUTION	Position 7C

Resolution

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set oscilloscope sweep to view horizontal information.

3. Set the oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect the oscilloscope external sync connector to the H Drive source. Synchronize the oscilloscope externally, negative slope.

5. Select the VIDEO function at the front panel.

6. Compare oscilloscope display to Figure 19a (page 59).

7. The Resolution pattern segment is presented as a "multiburst" of various resolution densities. Each burst is separated by a 50% gray level to aid in visual observation of the signal on the oscilloscope and of the pattern as displayed on a monitor.

   Each burst may be adjusted independently to the modulation repetition rate desired to develop the t.v. lines resolution required. The burst frequency or repetition rate, is adjusted in performance verification of the RESOLUTION test pattern. Refer to that procedure (page 123) for individual burst performance test if desired. Rep Rate 1 is the coarsest resolution (at lowest repetition rate), usually the first burst appearing at the left edge of the television raster.

Usually succeeding bursts are adjusted to progressively higher repetition rates so that the fifth and final burst (Rep Rate 5) contains the highest resolution content to be used. This places the finest detail near the center of the television raster where best display performance usually is obtained. Any other sequence of resolution rate presentation may be used including all bursts at the same rate. However, it is still necessary to calibrate each individual burst using its own individual potentiometer, as detailed in the RESOLUTION function procedure (page 123).

8. This completes performance verification of the Resolution segment of the Video signal.

Black Reference

1. Inspect the Black Reference portion of the Video test pattern.

2. Compare oscilloscope waveform to the Black Reference segment of the Video signal as shown in Figure 19a (page 59).

3.* The whiter-than-black pulse of the Black Reference segment is to be adjusted to the same level as the pedestal setup (nominally 0.039v.) by use of the White/Black Level control at the left side on the GRAY SCALE (Position 4B) circuit card.

4. Observe the video portion of the output composite video signal. The sync and blanking portions of the composite video signal are clocked and not adjustable.

5. This completes performance verification of the Black Reference portion of the Video signal.

Gray Scale

1. Inspect the Gray Scale segment of the Video signal on the right half of the horizontal scanning line.

2. Set the Channel 1 input amplitude sensitivity at 0.2v. per division. Oscilloscope sweep rate should show the entire horizontal line when using horizontal related sync and observations.

3.* Using the Uncal control at the oscilloscope input, reduce pattern amplitude so that the first step of Gray Scale (not including the blanking pedestal) is positioned at the center graticule on the oscilloscope grid. The tenth level (white) should then be positioned at the 0.9v. grid line.

4. Check that there is a linear staircase presentation with steps of uniform level; one level will be on each minor graticule division on the oscilloscope grid. If there is any deviation from Figure 19a (page 59), performance verification should be performed as detailed in the GRAY SCALE function procedure (page 117). If other than a linear stairstep presentation is desired, a revised procedure should be followed which will obtain that presentation.

5. Observe the video portion of the output composite video signal. The sync and blanking portions of the composite signal are clocked and not adjustable.

6. This completes performance verification of the Gray Scale portion of the Video signal.

VIDEO

1. The procedure just outlined involves the composite G (green) channel only. The R (red) and B (blue) channels contain the same video pattern signal. Check that the Composite Video R and Video B Outputs are identical to the Composite Video G Output.

2. TTL video R (red) and B (blue) channels contain the same video pattern signal as the TTL video G (green) channel. Check that the TTL Video R and B Outputs are identical to the TTL Video G Output.

3. Observe the composite video portion of the signals; video, blanking and sync portions should remain at the levels set in Video Signal Verification (page 106).

4. Observe the TTL video portion of the signal. The video portion should remain at the levels observed in Video Signal Verification (page 106). Blanking and sync portions of the TTL signal will not be present.

5. Connect the Video Output to the monitor to display the Video test pattern. The Resolution, Black Reference and Gray Scale segments should appear straight, and extend from top to bottom of the display without interruption.

6. Performance verification of the Video test pattern is now complete.

COMBINATION

The Combination test pattern consists of the Video pattern plus Color Bars in one raster simultaneously. These individual functions should have been verified prior to selection of the Combination test pattern. A strip of Video appears through the Color Bars segment of the Combination pattern at approximately 20% raster height. The height of the Video portion can be adjusted per user's discretion by programming changes. Note that the Video portion of the Combination pattern is monochrome and the Color Bars segment is displayed in RGB color. The Combination test pattern is developed by the following circuit cards:

4000	GRAY SCALE	Position 4B
4007	GRAY SCALE SELECT	Position 5B
4001	VIDEO CLOCK	Position 6B
4002	RESOLUTION CONTROL.	Position 7B
4006	PATTERN LOGIC	Position 9B
2155	TTL VIDEO R	Position 3C
2155	TTL VIDEO G	Position 4C
2155	TTL VIDEO B	Position 5C
4008	CLOCKED COLOR BAR	Position 6C
4013	RESOLUTION	Position 7C

Video

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set oscilloscope sweep to view horizontal information.

3. Set the oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect the oscilloscope external sync connector to the H Drive source. Synchronize the oscilloscope externally, negative slope.

5. Select the COMBINATION function at the front panel.

6. Compare oscilloscope display to Figure 20 (page 61).

7. The Resolution pattern segment is presented as a "multiburst" of various resolution densities. Each burst is separated by a 50% gray level to aid in visual observation of the signal on the oscilloscope and of the pattern as displayed on a monitor.

   Each burst may be adjusted independently to the modulation repetition rate desired to develop the t.v. lines resolution required. The burst frequency or repetition rate, is adjusted in performance verification of the RESOLUTION test pattern. Refer to that procedure (page 123) for individual burst performance test if desired. Rep Rate 1 is the coarsest resolution (at lowest repetition rate), usually the first burst appearing at the left edge of the television raster. Usually succeeding bursts are adjusted to progressively higher repetition rates so that the fifth and final burst (Rep Rate 5) contains the

highest resolution content to be used. This places the finest detail near the center of the television raster where best display performance usually is obtained. Any other sequence of resolution rate presentation may be used including all bursts at the same rate. However, it is still necessary to calibrate each individual burst using its own individual potentiometer, as detailed in the RESOLUTION function procedure (page 123).

The Black Reference segment appears at the center of the Video test pattern and is composed of three vertical strips of video at or near black level with maximum contrast, white reference levels at the left and right sides of the display. The whiter-than-black pulse was adjusted previously in the VIDEO function procedure (page 128).

The Gray Scale portion is presented in the right half of the television line. Check that there is a liner staircase presentation with steps of uniform level.

Using the Uncal control at the oscilloscope input, reduce pattern amplitude so that the first step of Gray Scale (not including the blanking pedestal) is positioned at the center graticule on the oscilloscope grid. The tenth level (white) should then be positioned at the 0.9v. grid line.

One level of the Gray Scale should appear on each minor graticule division on the oscilloscope grid. If there is any deviation from Figure 20 (page 61), performance verification should be performed as detailed in the GRAY SCALE test procedure (page 117).

8. Height of the Video portion of the Combination test pattern was programmed (usually to provide a height of 20% of the active horizontal time, as shown in Figure 20) initially when scan rates were programmed at the APL START (Parameter 32) and APL STOP (Parameter 33) prompts. As this horizontal strip is programmed to provide a height of 20%, the Video portion will start at approximately 40% down from the top of the raster and will stop at approximately 60% down from the top of the raster.

   Refer to the TO EXAMINE OR EDIT (MODIFY) PARAMETERS IN A SCAN RATE PREVIOUSLY STORED flow chart (page 87) for proper editing procedure, if it is necessary to edit start and stop of the Video segment.

9. The procedure just outlined involves the composite G (green) channel only. The R (red) and B (blue) channels contain the same video pattern signal. Check that the Composite Video R and Video B Outputs are identical to the Composite Video G Output.

10. TTL video R (red) and B (blue) channels contain the same video pattern signal as the TTL video G (green) channel. Check that the TTL Video R and B Outputs are identical to the TTL Video G Output.

11. Observe the video portion of the output composite video signal. The sync and blanking portions of the composite video signal are clocked and not adjustable.

12. Observe the TTL video portion of the signal. The video portion should remain at the levels set in Video Signal Verification (page 106). Blanking and sync portions of the TTL signal will not be present.

13. This completes performance verification of the Video segment of the Combination test pattern.

Color Bars

1. Adjust oscilloscope sweep to inspect the Color Bars portion of the Combination test pattern.

2. Compare oscilloscope display to the Color Bars segment of the Combination signal as shown in Figure 20 (page 61).

3. Check that one complete cycle of color bars (green component) is presented in the active horizontal scanning line length as shown in Figure 20. The Color Bars segment is clocked and not adjustable.

4. Check that two complete cycles of color bars (red component) is presented in the active horizontal scanning line length when the oscilloscope input is connected to the Composite Video R Output connector at the rear panel.

5. Check that four complete cycles of color bars (blue component) is presented in the active horizontal scanning line length when the oscilloscope input is connected to the Composite Video B Output connector at the rear panel.

6. If there is any deviation of the Color Bars segment from Figure 20 (page 61), refer to the COLOR BARS performance verification procedure (page 126).

7. TTL video R (red), G (green) and B (blue) channels are identical to the composite video R, G and B channels, without blanking or sync.

8. Observe the composite video portion of the signal; video, blanking and sync should remain at the levels set in Video Signal Verification (page 106).

9. Observe the TTL video portion of the signal. The video portion should remain at the levels observed in Video Signal Verification (page 106). Blanking and sync portions of the TTL signal will not be present.

COMBINATION

1. Connect the Video Output to the monitor to display the Combination test pattern. In the Video portion of the Combination test pattern, the Resolution segment should appear in the left half of the television line, the Black Reference segment at the center, and the Gray Scale should appear in the right half of the television line. The Video segment will be positioned on the raster as programmed.

   If a color monitor is used, vertical bars of various colors should be obtained for the Color Bars segment of the Combination test pattern. If a monochrome monitor is used, look at each segment component individually in which there will be black and white bar patterns of different repetition rates, showing one cycle for green, two cycles for red, and four cycles for blue.

2. Performance verification of the Combination test pattern is now complete.

CHARACTER

This function provides horizontal rows of the Character Cx on the display screen, The characters are of the 5 x 7 pixel format, which means the character, when properly programmed, will be of five-to-seven width-to-height ratio. Characters are developed in a 10 x 10 pixel matrix, meaning that characters will be spaced five pixels apart (100% separation between characters) in the horizontal display plane and spaced apart by three scanning lines in each field of the vertical plane. The clock frequency can be varied to adjust the number of characters per row. The number of rows is determined by the number of scan lines per field. The characters can be displayed in a number of ways as illustrated in Figures 21 and 22 (page 63). Circuit cards involved include:

4014	CHARACTER	Position 8C
4013	RESOLUTION	Position 9C

1. Connect the video coax cable to the Composite Video G Output connector and oscilloscope Channel 1 input, terminated.

2. Set oscilloscope sweep rate to view horizontal information.

3. Set the oscilloscope Channel 1 input amplitude sensitivity at 0.5v. per division.

4. Connect the oscilloscope external sync connector to the H Drive source. Synchronize the oscilloscope externally, negative slope.

5. Set the Function Selector switch at CHARACTER.

6. Select the 100% or 50% mode, as desired, by installing jumper A-B for 50% duty cycle or jumper B-Y for 100% duty cycle on the CHARACTER circuit card in Position 8C.

7. Connect the Video Output to the monitor to display the Character test pattern. Compare monitor display to Figure 21 (page 63). The display should contain rows of white characters on a black background. The character can be either 100% or 50% duty cycle, as shown in Figures 21a and 21b. Use a magnifying glass to inspect the character height, which should span seven scan lines in each field (fourteen lines will be intensified in the 2:1 interlaced raster). Measure the character height and width to verify the height/width ratio to be 7:5.

8. Determine the character spacing and compute the number of characters per line being developed in the horizontal active line time for the scan rate in use.

9.* The number of characters generated in each horizontal row across the display screen can be adjusted by use of the Character Clock control located at the right side of the RESOLUTION circuit card in Position 9C.

10.* Adjust the space between Character pattern elements to match width of these pattern elements by use of the Character Balance control located at the left side on the RESOLUTION circuit card in Position 9C.

11. Figure 22 (page 63) displays the Character function in a non-interlaced raster. This can be obtained by entering an even number of scan lines per two fields at Parameter No. 1, NO. LINES.

    Refer to the TO EXAMINE OR EDIT (MODIFY) PARAMETERS IN A SCAN RATE PREVIOUSLY STORED flow chart (page 87) for proper editing procedure if it is necessary to re-program a scan rate for a non-interlaced raster.

12. The procedure just outlined involves the composite G (green) channel only. The R (red) and B (blue) channels contain the same video pattern signal. Check that the Composite Video R and Video B Outputs are identical to the Composite Video G Output.

13. TTL video R (red) and B (blue) channels contain the same video pattern signal as the TTL video G (green) channel. Check that the TTL Video R and B Outputs are identical to the TTL Video G Output.

14. Observe the composite video portion of the signal; video, blanking and sync should remain at the levels set in Video Signal Verification (page 106).

15. Observe the TTL video portion of the signal. The video portion should remain at the levels observed in Video Signal Verification (page 106). Blanking and sync portions of the TTL signal will not be present.

16. Performance verification of the Character function is now complete.

TROUBLESHOOTING

The Model 2501 Programmable Test Pattern Generator has been designed to provide the greatest reliability possible in the normal laboratory environment. Unfortunately some components, particularly capacitors and semiconductors, exhibit a limited lifetime, and lead to the possibility of component failure. In this instrument the components are derated to assure the longest possible lifetime; proper operation should be expected for at least a five year and probably ten year period.

Be sure to check the performance verification procedure to establish that failure has occurred definitely. Often a symptom of difficulty can be traced to improper adjustment of the unit.

Failures which would occur relatively early, within one to two years, are most likely due to semiconductor (integrated circuit) failure due to internal contamination at the time of manufacture or due to defective solder joints in assembly. Failures occurring at later times statistically would be attributed to electrolytic capacitor failure due to internal chemical reaction, etc.

In rare instances, there may appear in this equipment a deviation from the part as called out on the schematic and in the parts list. This is especially true in the case of semiconductor devices, diodes and transistors, where a number of types are interchangeable. The right is reserved to make use of interchangeable components where such substitution will provide equal or superior performance to that specified. It is suggested that if replacements are required, the type specified in the parts list be procured.

You are urged to read the instruction manual completely before connecting the unit for operation. Observance of only a few procedures will provide greater operator convenience and will assure most effective application of the equipment as well as provide maximum safety to the user.

CAUTION

Even low voltages commonly present in transistorized circuits are potentially dangerous. Additionally full line voltage is present on fuse terminals, power switch terminals, and other exposed points within the interior of the unit, and are accessible when the cover of the equipment is removed. Caution should be exercised, as follows:

a. Remove power by unplugging the line cord when removing covers and inspecting interior of the unit.

b. Observe the common safety practices when servicing equipment (dry skin, insulation of the body from ground, etc.).

c. Never work on electrical equipment when alone. Service and calibration should be attempted only by a qualified electronics technician.

Fault isolation can be achieved most efficiently by determining the circuit card module causing difficulty, from symptoms in the output waveforms.

Check that the output signals conform to typical waveforms. If there is a problem in one of these signals, troubleshoot the proper section. All synchronizing and timing pulses are developed in the computer sync generator section. The patterns are developed from either 20H or 40H clocks from the computer with logic on the separate functional cards providing the desired signal. If there is a fault in the video and all sync pulses are normal, troubleshoot the test pattern section. Lack of a proper output signal level can usually be traced to problems in the power supply or related chassis problems.

Programmable Sync Generator Section

a. Lack of all pulses can be traced to failure of the 20 mHz clock generator, power supply difficulties, or a basic problem in the computer logic.

   A loss of all outputs but presence of the +5v. would indicate that the master oscillator located on the H SYNC GENERATOR (2195) circuit card has failed. If the display indicates correct timing but horizontal pulses appear in error on the oscilloscope, this would indicate that the master oscillator is running at an incorrect frequency, not the 20 mHz as designed. Note that if an external master oscillator input (option) is used at other than 20 mHz, display timing would not be accurate.

b. Apparent trouble in any one video level synchronizing waveform such as insufficient amplitude but correct timing, or no output, could be the fault of the PULSE OUTPUT (2003) or TTL PULSE OUTPUT (2118) circuit card. If it is verified that these cards are operating properly, check further as listed below.

   The video level pulse outputs are developed on the PULSE OUTPUT (2003) circuit card, which should be checked if pulse levels are not proper. The TTL level pulse outputs are developed on the TTL PULSE OUTPUT circuit card (2118), which should be checked if these pulse levels are not correct.

c. The uP INTERFACE circuit card processes information from the computerized sync generator to the sync output cards located in the pattern generator section.

d. The computer sync generator works from a switching power supply mounted on the POWER INTERFACE card (2201) which supplies +5v. to this circuit section. This power supply should be checked upon complete failure of the instrument.

e. If all horizontal rate pulse widths appear to be in error, including total horizontal line time, the end of line counter clear on the H SYNC GENERATOR circuit card* (2195) may be malfunctioning. Correspondingly, a jitter in the horizontal pulses would indicate that the end of line clear is not stable, typically providing a 50 nsec. jitter from one line to another.

f. If individual horizontal rate pulse widths appear to be in error, as displayed but not as programmed, this indicates a slow down in the access time to the random access memories. Such a failure would be most likely caused by heat build up in which case ventilation should be checked.

g. If all vertical rate pulses appear to be in error, the end of field counter clear on the V SYNC GENERATOR (2192) circuit card* may be malfunctioning.

h. If any one horizontal or vertical pulse width appears to be other than programmed, the most likely cause is a software error in the microprocessor located on the CPU SYNC GENERATOR (2190) card.

i. Appearance of the "bad write" error codes indicate a probable bad EEPROM on the V SYNC GENERATOR (2192) board*. Code numbers 1 through 34 indicate EEPROM U25 is at fault, while numerical code 35 through 68 indicates failure in EEPROM U26. If an error is encountered in the lower memory, the fault can be verified by attempting to store the program data in the upper memory, or vice versa.

j. Error code "HELP I AM BROKE" requires consultation with the factory. When this error code appears and the ENTER button is pushed, error code numbers will be displayed. Typically, this will present a 12 digit number plus AE, indicating an address error within the computer. The presence of a 12 digit code plus BE indicates a bus error in which the system is trying to store information in a non-existent location.

k. The presence of horizontal pulses only, vertical pulses only or no output but the master oscillator has been confirmed to be operating properly and the display is normal, indicates that the parallel port (68230 on the V SYNC GENERATOR circuit card*, 2192) has not enabled counters.

l. No display would be a fault in power from the KEYBOARD INTERFACE (2194) card or the serial communication from the CPU SYNC GENERATOR card (2190) to the keyboard/display sub-assembly. A ribbon cable is used for this communication, and should be checked in this type of fault.

m. If there is no keyboard action, erratic entry, or wrong numbers entered, this indicates a keyboard problem. If the keyboard is verified to be good, the communication is controlled by the DUART 68681 on the CPU SYNC GENERATOR (2190) card. This should be checked for keyboard problems after keyboard quality has been verified.

*H/V MPU CONTROLLED SYNC GENERATOR (2221) may be used in place of both the H SYNC GENERATOR (2195) and V SYNC GENERATOR (2192) circuit cards.

Test Pattern Generator Section

Should malfunction occur, fault isolation is effectively achieved by the following procedure:

1. Inspect the video output for conformance to typical waveforms as shown in previous sections of this manual. If there is a fault in basic timing in all patterns or in the blanking or sync signals, the difficulty is in the programmable sync generator section which must be corrected before troubleshooting can be performed on the pattern generator section.

   Inspect the H Drive, V Drive, Blanking and Sync outputs for conformance to typical waveforms as shown in previous sections of this manual.

2. The video level (amplitude) control voltage is developed on the VIDEO CONTROL (4010) circuit card. Therefore, the video will remain at zero (0v.) level if this card is removed. It must be installed to obtain the basic Flat Field video signal output.

3. All patterns except Character are developed from pattern clocks developed in the programmable sync generator. The Video test pattern is generated from a 40H clock; the Gray Scale, Window, Bars, Dots, Color Bars and Resolution patterns employ a 20H clock. If difficulty exists in all patterns for a particular clock rate, check pattern clock outputs from the sync generator section.

4. If difficulty is noted in a certain pattern, check for proper operation at other functions. Problems can be isolated to the particular circuit card modules used for that particular pattern. If a problem is apparent in more than one pattern, remove modules selectively until proper operation is obtained at other functions, as follows:

   Bars and Dots . . . . . CLOCKED BAR/DOT (4003) circuit card

   Gray Scale . . . GRAY SCALE (4000) and GRAY SCALE SELECT (4007) circuit cards

   V Stripe and Window . . . . . PATTERN LOGIC (4006) circuit card

   Resolution . . . RESOLUTION CONTROL (4002) and RESOLUTION (4013 in Position 7C only) circuit cards

   Color Bars . . . . . CLOCKED COLOR BAR (4008) circuit card

   Video . . . . . VIDEO CONTROL (4010), GRAY SCALE (4000) and RESOLUTION (4013 in Position 7C only) circuit cards

Combination . . VIDEO CONTROL (4010), GRAY SCALE (4000), RESOLUTION (4013 in Position 7C only) and CLOCKED COLOR BAR (4008) circuit cards

Character . . . CHARACTER (4014) and RESOLUTION (4013 in Position 9C only) circuit cards

Difficulties associated with no video portion of signal or improper video level will originate either in the POWER REGULATOR (2110), VIDEO CONTROL (4010) or TTL VIDEO (2155) circuit cards.

The RESOLUTION card is emitter-coupled to the TTL VIDEO cards (distributed to three TTL VIDEO cards in RGB color units by emitter follower circuits on the CLOCKED COLOR BAR card). A problem on the RESOLUTION card may force all video to black level, resulting in an apparent loss of video while sync and blanking remain at the output. Check for this possibility by removing the RESOLUTION card in Position 7C. Other generator functions should operate normally. Note that the CLOCKED COLOR BAR card must be installed to check Resolution.

The Gray Scale signal is processed through the VIDEO CONTROL card to the TTL VIDEO circuit cards. For other functions, this signal path carries the video "white" level, serving as a clipper type gain control.

5. Improper pattern generation, amplitude, phase ripple or hum, inaccurate sync timing, etc., of an extreme nature can be traced generally to low line voltage, misadjustment or failure of the POWER REGULATOR (2110) circuits.

Operation of each of these cards is discussed in detail under CIRCUIT DESCRIPTION (page 151); refer to the appropriate paragraphs after fault isolation as described above.

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ACCESSORIES AND SERVICE

Vii Test Equipment is designed for long, reliable service under adverse operating environments. It should require a minimum of maintenance or service if properly applied.

A number of accessories are available for extended operation of Vii Test Equipment, including special housings, cables, etc. especially designed to suit unusual requirements. Special configurations of Vii Test Equipment are available for integration into existing or contemplated systems, such as units without cases, special accessory functions brought to the front panel, etc.

Vii stands ready to assist in advising as to proper application of its products, to aid in calibrating and servicing instruments, and to help in integrating our products into your system for maximum of utility.

Vii provides factory calibration and repair service. Charges are based upon the prevailing hourly rate for labor, cost of parts, and transportation to and from Vii facilities. Please contact the factory for further information. To provide a most accurate quotation (or estimate for repairs) you must supply the MODEL NUMBER, SERIAL NUMBER and PRODUCTION SERIES letter.

A RETURN AUTHORIZATION IS REQUIRED. Instruments received without prior authorization will not receive attention. Incoming shipments must be prepaid unless prior arrangements have been made. Unanticipated arrivals with freight C.O.D. WILL BE REFUSED. Account arrangements must be complete before repairs can proceed, including receipt of a confirming copy of relevant purchase orders.

To obtain a return authorization, or other information related to these services, contact:

VISUAL INFORMATION INSTITUTE, INC.
ATTN: SALES COORDINATOR
719 LOWER BELLBROOK ROAD
XENIA, OH 45835
Phone: (513) 376-4361

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MAINTENANCE

Vii Test Equipment has been designed to operate for long periods of time without the need for frequent attention. As with any laboratory equipment, periodic performance verification and calibration as found to be required, on a regular schedule, is of value. In most ordinary applications, performance verification is suggested at six month intervals. If the instrument is being used as a reference standard, performance verification at three month (90 day) intervals may be more appropriate.

Instruments which use a cooling fan require periodic cleaning to remove dirt that has blown in and has collected on internal parts. A dust/dirt collection on parts that depend upon circulated cooling air can insulate those parts so that they are not properly cooled. Therefore it is suggested that the cooling fan and instrument interior be checked monthly and cleaned as necessary.

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LIMITED WARRANTY

Vii Test Equipment is guaranteed to be free of defects in material and workmanship for a period of one year from date of shipment, when operated in accordance with the instructions and specifications provided. Such limited warrant is made in lieu of any other guarantee or warranty, expressed or implied, and is offered only to the original purchaser. If such defects are confirmed through our inspection, the product will be repaired or replaced, at our option, without charge to the purchaser for parts or for labor. This warranty does not cover damage which occurs in shipment or due to misuse or abuse of the apparatus, and is not applied to cables or decorative, stained or painted finishes.

Those requesting adjustment through the terms of this warranty are instructed to contact the factory for authorization to return the equipment before shipment. Items for which authorization is issued are to be sent prepaid.

Vii Test Equipment is designed and constructed using the most effective and safest industrial practice known, and in accordance with printed and accepted practices for fabrication of industrial electronic equipment. Inasmuch as Visual Information Institute, Inc. has no control over the manner in which the equipment will be interconnected, the corporation cannot and does not assume any liability for circumstances or damages arising from use of this equipment.

This warranty does not apply to equipment which has been modified in any way to other than the original factory configuration.

CAUTION

When removing and replacing jumpers on printed circuit cards, do not overheat card and lift printed circuit card copper pads. Use a vacuum device to remove solder before existing jumper is removed. Jumper removal and replacement must be done by those experienced with printed circuit cards. Damage to printed circuit cards caused by improper methods will void the warranty.

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MODIFICATIONS

This section contains a description of modifications or changes to instruments to conform to a particular customer's request or to correct documentation to include late revisions in circuitry configuration or components included to improve performance of the instrument.

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CIRCUIT DESCRIPTION

The Model 2501 Programmable Television Test Pattern Generator is a self-contained instrument which develops precise reference television test signals. All signals are synthesized through modern digital techniques; all circuits are completely transistorized, composed mainly of multivibrators which employ high speed switching transistors. Power supplies are closely regulated to insure dependable, stable operation over wide variations in ambient conditions. The unit is modularized; all circuits are contained on fiberglass plug-in cards. The design is such that functions may be described by individual circuit card discussion.

The basic chassis is composed of vertical card files which contain power regulator and pattern development circuit cards. The rear of the cabinet contains power regulators and transistors mounted on a heat sink, the power transformer, power cord connector, video and synchronizing connectors, and a terminal block for transformer connections. The front card file contains an internal, computerized sync generator.

Power Regulation

Separate power supplies are employed for the computerized sync generator and video pattern circuitry. The sync generator section operates from a switching power supply module mounted on the POWER INTERFACE (2201, Position 20) circuit card in the sync generator card cage; this module is not considered repairable, and should be replaced if difficulty is found in the +5v. supply in the computer section.

Video and pattern logic circuits develop "clean" signals which, in turn, demand power sources with very low ripple and absolutely no noise as might be present in a switching type power supply. Therefore, conventional rectifiers and regulators are used which operate at the power input frequency.

The POWER REGULATOR circuit card (2110, Position 3C) includes voltage regulator circuits to develop +12v., +5v., +8v. and -5v. voltages. Four separate regulators are employed: one for +12v. (non-adjustable), one for +8v. (non-adjustable), one for -5v. (non-adjustable) and an adjustable +5v. regulator with ultra-low ripple for voltage controlled oscillator operation. The +12v., +8v. and -5v. regulators are located on a heat sink mounted to the cabinet. The +5v. rectifier diodes, power transistors for the adjustable +5v. regulator and auxiliary negative voltage level also are located on the heat sink. The heat sink assembly also contains a power transistor to develop a high current -4.3v. (nominal) voltage from the -5v. source.

Three separate rectifiers, each full wave, are used. The +8v., +5v. and -5v. supplies operate from the same transformer with diode polarity providing either positive or negative d.c. voltages as desired.

Diodes CR1, CR2 and filter capacitor C3 develop a d.c. level of about +17v., reduced by Positive Regulator Z1 on the rear panel heat sink to +12v. This rectifier is kept lightly loaded to keep ripple valleys well above possible regulator dropout levels.

Diodes CR3, CR4 and filter C7 on the rear panel heat sink develop a negative voltage of about -12v. which is reduced by negative regulator Z3 to -5v.

Diode rectifiers CR1 and CR2 are located on the rear panel heat sink for the main +5v. supply d.c., as this supply has a large current capacity. The rectified voltage from the diodes and filter C7 is connected to the collector of the power transistor for this supply which is mounted on the heat sink attached to the cabinet. The regulated +12v. is used as a reference to operate a precise, low ripple (1 mv or less) +5v. regulator to operate voltage controlled astable multivibrators which develop test pattern circuit elements. Regulator circuitry is located on the POWER REGULATOR circuit card. The +12v. d.c. level is submitted through dropping resistor R4 to zener diode CR5, temperature compensated at the optimum zener level, 3.6v. This reference level is routed through an adjustable voltage divider R1, to one side of a "long-tailed pair" circuit. The adjustable voltage at the base of Q3 develops a reference level through the emitter of Q3 to resistor R5. The +5v. level is fed back into the base of Q2. Therefore a base-to-emitter bias level for Q2 is established, controlling the current through load resistor R6. This, in turn, controls the collector voltage for amplifier Q2, which feeds a controlling level from the base of Q1 to the base of a power regulator transistor mounted on the cabinet. From the emitter of the power transistor Q1, 2N3053, voltage is distributed throughout the unit, and is returned to the POWER REGULATOR circuit card as a reference and for filtering to C5. The result is a very precise +5v. reference level which exhibits less than 1 millivolt ripple.

Programmable Sync Generator Section

The programmable sync generator develops all synchronizing pulses from a central clock. This insures absolute stability of signals, yet flexibility is maintained through the use of programmable elements, EEPROMS. A separate circuit card is provided for pulses to be developed at horizontal and vertical rates; the signals such as sync and blanking which combine horizontal and vertical components mixed together are developed on the vertical rate circuit card. All operations on these cards are controlled by a microprocessor on another circuit card. Pulses are processed for routing out of the generator on an interface card, and a +5v. switching power supply for all sync generator operations is located on another circuit card.

There is a great diversity of scan rates used in television systems and display devices at this time. To accommodate all as efficiently as possible, horizontal rate synchronizing pulses are developed with a standardized 0.1 usec. (100 nsec.) timing increment. This allows all rates to be developed from a very stable reference clock. Otherwise it would be necessary to customize master oscillator clock frequency for each scan rate which would imply complete raster redesign for each rate encountered. The timing increment of 0.1 usec. has proven to be acceptable for nearly all applications.

The time based HORIZONTAL SYNC GENERATOR card (2195, Position 18) develops all pulses from a precision clock oscillator which operates at 20 mHz. Pulses from this component are used to clock all raster operations. The HORIZONTAL SYNC GENERATOR contains a 20 mHz oscillator which serves as a master clock for horizontal rate pulse generation. Transistor Q3 serves as an on-off control for the option of an external clock. To use the internal clock, +5v. is applied (by the rear panel switch if the external option is included) to Pin 1 of P2. Oscillator Y1 is energized and Q3 saturates. As no voltage is applied to Q2, gate U25A allows the 20 mHz to pass through to U25D for distribution. The 20 mHz signal is used only on this circuit card.

A separate random access memory (RAM) is used for each horizontal rate parameter, type 2147H, 4K x 1. Parameter assignment is as follows:

U1 - H Blanking	U5 - V Bar Clock	U9 - 40H Pattern Clock
U2 - H Drive	U6 - 2H Serrations	U10 - H Gate
U3 - H Sync	U7 - 2H Equalizing	U11 - H Window
U4 - H Trigger	U8 - 2H Clock	U12 - End of Line (EOL)

Memory outputs are routed through type D flip-flops, U13 and U14, where the RAM data is latched to the 20mHz clock. These type D latches are 74F74, a very fast component that can respond within the 50 nsec. of one clock cycle. All pulses, except the End of Line (EOL) command are routed out of the card for processing elsewhere.

All other circuitry on this card is used to communicate with the random access memory, loading into them what values are programmed by the keyboard through the CPU SYNC GENERATOR card. Basically the horizontal rate sync generator system is a binary counter with up to 2048 count capacity, with the count selected for any one parameter stored in the RAM as commanded. Therefore the system can develop up to a 204.8 usec. horizontal line time although the software program is limited to 204 usec. as being the longest horizontal line in common use at this time.

RAM communication with the CPU SYNC GENERATOR card is handled through buffers U18-U20. They reshape pulse information from the MBA PROGRAMMABLE SYNC circuit card and serve as an isolation for binary counters U15-U17. These counters select the location in the RAM which the CPU will write to to store parameter data. The CPU is allowed to write to the RAM whenever the Horizontal Enable (HEN, P2, Pin L) is low. Then, when a clock edge is received at Pin 2 of U15, U16, and U17, these counters clock data which is on Pins 3, 4, 5 and 6, acting as a latch. This four bit address selects the RAM which is to accept the data and inserts the data. Components RP1 and RP2 are merely series resistors which serve to filter these very fast signals, eliminating noise which might cause a fault in data loaded into the RAM.

Comparator U23, 8 bit, compares the address line A14, A15, A16 through A19 and the address strobe AS inputs to the jumper matrix J1. If they match, the software program is appropriate for this circuit card, and this card is selected to receive data. Thus the bi-directional transceiver U21 is enabled and can communicate with the identical transceiver on the CPU SYNC GENERATOR card. If the READ/WRITE command which originates in buffer U20 is at high level, data is transferred (read) from Pin 2 to Pin 18 of U17. If the command is low, data is transferred from Pin 18 to Pin 2. Note that only the "write" function is used in this particular application.

The SEL command from Pin 19 of U23 also is inverted by gate U25C and routed to shift register U24, 74S164. When the shift register at Pin 6 goes high, transistor Q1 saturates; the BDTACK command goes low, routed out of this card to the CPU SYNC GENERATOR card, signaling it that either data has been accepted or that a writing sequence is complete. Pins 1 and 2 of U24 are reserved for design and production test.

The VERTICAL SYNC GENERATOR (2192, Position 17) circuit card develops all vertical rate pulses and also processes certain horizontal rate pulses to develop "composite" signals, Blanking and Sync. Operating philosophy is identical to that of the horizontal rate card discussed above. This card also contains the EEPROMS where raster information is stored.

Components U6, U7 and U8 are 4K x 4 static random access memories (RAM) which are the "working" memory for the vertical rate pulses. They must be specially buffered by U9 and U10 because the static RAM is an "in-out" type which must be made uni-directional rather than bi-directional in this application to prevent data feedback to the motherboard bus. Basically data from the motherboard bus is buffered by U17 for board distribution then by U9 and U10 for RAM isolation. The data from U9 and U10 is routed to the control inputs of the static RAMs, Pins 12, 13, 14 and 15. Data address is provided to the RAMs by binary counters U3, U4 and U5; the binary counters operate from data provided by buffers U14 and U15. The counters operate from the V clock, which is at 2H rate, except when the vertical section is being written by the CPU SYNC GENERATOR card, at which time the CPU system clock rate is used. Counters are reset by the End of Field command to reinitiate the sequence for each two fields of the video raster.

Gates U18C and U18D develop the $\overline{EN4}$ and $\overline{EN3}$ signals, respectively, which are used to enable buffers U9 and U10 when information is being written to the RAM. The selection may be for U6, U7 or U8 alone as needed for the particular type of data to be stored. The assignment is:

U6 - V Blanking, V Drive, V Window, End of Field
U7 - V Front Porch, V Sync, V Post, V Trigger
U8 - H Bar, H Crosshair, APL Gate, V Gate

The U18C and U18D gates operate from the VEN data generated in U24, a Parallel Interface Timer (PIT).

Data from the RAMs is routed to type D flip-flops U11, U12 through the in/out bi-directional ports, Pins 12, 13, 14 and 15, where the actual vertical rate pulses are developed. Flip-flop U11 operates from the V clock, while U12 operates from the 2H rate serration pulse to properly phase the V sync pulse at Pin S. Pulses which do not require further processing, such as V drive, are routed to output connector P2. Those which are to be processed further are sent to programmable logic arrays U1 and U2. Here various signals are mixed to assemble the specific pulse trains such as Blanking and Sync which contain both horizontal and vertical rate data (U1) and various "housekeeping" control data (U2).

Programmed information is stored in EEPROMS U25 and U26. Data is obtained from buffers U14 and U15; the storage operation is controlled by flip-flop U21. Two EEPROMs are used to obtain sufficient storage capacity for 68 raster formats. Each format is assigned an access number; 1 through 34 are stored in U25, 35 through 68 in U26. The EEPROMs require several commands for read and write operations:

1. The EWE (EEPROM While Enable) command (to Pin 21 of the EEPROMs), generated by U21, must be at a low level for the EEPROM to be written to; storage of a byte in one location requires 10 msec. Therefore to store one raster, time required is 2048 x 10 msec. While the EWE command is low, the address and data are internally latched and cannot change. When the EWE command returns to high level, the next storage command is received from the CPU SYNC GENERATOR card, EWE goes low, and the process is repeated. The EWE pulse is generated by U21 as commanded by the ESTB signal from Programmable Logic Array (PAL) U1; the ESTB is a combination of the R/$\overline{W}$ (Pin 4) and EPROM select (Pin 15) signals in the PAL.

2. The EOE (EEPROM Output Enable) command allows an EEPROM to be interrogated, or read, when a raster format is requested. The EOE command is developed by PAL U1, and is a combination of the "read" and EPROM select signals.

3. While EEPROM will be read or written to is determined by the EPR1 and EPR2 signals developed by gates U27C and U27D, combination of address command A11 and the EPROM signal from PAL U1.

There are many "housekeeping" functions to support the circuit operations described above. Comparator U20, 8 bit, compares the address line A14, A15, BA16 through BA19 and the address strobe AS inputs to the jumper matrix J1. If they match, the software program is appropriate for this circuit card, and the comparator output at Pin 19 goes low (SEL) instructing other components that this card is selected to receive data. Thus the bi-directional transceiver U17 is enabled and can communicate with the identical transceiver on the CPU SYNC GENERATOR card. If the READ/WRITE command which originates in PIT U24 is at high level, data is transferred (read) from Pin 2 to Pin 18 of U17. If the command is low, data is transferred from Pin 18 to Pin 2. Note that only the "write" function is used in this particular application.

The SEL command from Pin 19 of U20 also is routed to gate U18B and routed to shift register U13, 74S164. The clear pulse to Pin 9 of U13 is processed through gates U18A and U18B, the $\overline{PIT}$ and $\overline{DS}$ signals added. This causes the internally generated BDTACK signal of U24 to be inhibited, locking out the Parallel Interface Timer so that shift register U13 can continue to run when anything else is selected on the board. When the shift register at Pin 6 goes high, transistor Q1 saturates; the BDTACK command goes low, routed out of this card to the CPU SYNC GENERATOR card, signaling it that either data has been accepted or that a writing sequence is complete. Pins 1 and 2 of U24 are reserved for design and production test.

The Parallel Interface Timer (U24) contains a total of 32 registers which control various outputs. Pins D0-D7, A1-A5, DTACK, RESET, READ/WRITE are inputs; all others are outputs. All are controlled by the CPU SYNC GENERATOR card signals routed through buffers U14 (A1-A5) and U17 (D0-D7). Outputs include:

VEN . . . Vertical Enable
HEN . . . Horizontal Enable
EPEN . . . EEPROM Enable

TEST . . .)
EXT . . .) not used in this
MISC . . .) application
BOUNCE . .)

The pulses not used on this card are routed to connector P2 for distribution on the MBA PROGRAMMABLE SYNC circuit card (2193). Outputs to U22 (Pins 4 - 11) are for a printer interface through connector J1 which possibly could be used for test and debug of the system, not used in this application. Inputs from U23 also are printer related, and not used.

The V blanking input at Pin 32 is used to develop the Bounce function, not used in this application.

The PIT signal on Pin 41 is used to select the appropriate EEPROM for storage or retrieval of data.

Sync format can be selected as any one of six modes (Broadcast, Industrial or Military as "standard" or "custom") controlled by the FC0, FC1 and FC2 signals routed to PAL U2.

An optional combination horizontal and vertical sync generator card, H/V MPU CONTROLLED SYNC GENERATOR (2221) can be used in place of the separate horizontal and vertical cards (2195 and 2192); the combination card can be placed in either Position 17 or 18 in the sync generator motherboard. The combination card contains four major sections -horizontal, vertical, pattern storage and control.

Horizontal rate information is processed by registers U1, U2 and U3, high speed RAMs U7, U8 and U9, high speed flip-flops U15 and U16, buffers U21 and half of U22, and various control gates.

The time based H/V MPU CONTROLLED SYNC GENERATOR card develops all horizontal rate pulses from a precision clock oscillator which operates at 20 mHz. Transistor Q1 serves as an on-off control for the optional use of an external clock. To use the internal clock +5v. is applied (by the rear panel switch if the external option is included) to Pin 1 of P2. Oscillator Y1 is energized and Q1 saturates. As no voltage is applied to Q3, gate U35A allows the 20 mHz to pass through to U35B for distribution. The 20 mHz signal is used only on this circuit card.

Each RAM, type IMS142, 4K x 4, can process four different pulses. The assignment is:

U7, Pin 12 = H Trigger	U8, Pin 14 = 2H Serrations
U7, Pin 13 = H Sync	U8, Pin 15 = V Bar Clock
U7, Pin 14 = H Drive	U9, Pin 12 = H Window
U7, Pin 15 = H Blanking	U9, Pin 13 = H Gate
U8, Pin 12 = End of Line	U9, Pin 14 = Pattern Clock
U8, Pin 13 = 2H Equalizing	U9, Pin 15 = 2H Clock

Memory outputs are routed through type D flip-flops, U15 and U16, where the RAM data is latched to the 20 mHz clock. These type D latches are 74F174, a very fast component that can respond within the 50 nsec. of one clock cycle. The edge triggered flip-flops U15 and U16 latch the data coming from the horizontal ram on the leading edge of HCLK which is the same edge that causes the horizontal counters to advance. All pulses, except the End of Line (EOL) command are routed out of the card for processing elsewhere.

All other horizontal section circuitry is used to communicate with the random access memory, loading into them what values are programmed into them by the keyboard through the CPU SYNC GENERATOR circuit card. Basically the horizontal rate system is a binary counter with up to 2048 count capacity with the count selected for any one parameter stored in the RAM as commanded. Therefore the system can develop up to a 204.8 usec. horizontal line time although the software program is limited to 204 usec. as being the longest horizontal line in common use at this time.

RAM communication with the CPU SYNC GENERATOR card is buffered by transceivers (transmitter-receivers) U21 and U22, which are enabled by gates U13C and U37B respectively. The direction of data transfer is dictated by command $\overline{WE}$; if $\overline{WE}$ is low the data is written into RAM, and read from RAM if $\overline{WE}$ is high. These buffers are isolated from the data bus during normal sync generator operation.

Counters U1, U2 and U3 are controlled by the HEN (Horizontal Enable) command. When the HEN goes high the counters are enabled. The counters U1 through U3 count from Ø to the location that EOL gives low. At that point they start the count again. EOL (End of Line) is the number of 50 nsec. pulses in the horizontal line. Components RP1 and R19-R22 are merely series resistors which serve to filter these very fast signals, eliminating noise which might cause a fault in data loaded into the RAM.

Counters U1-U3 are interrupted whenever the HEN command is in the "low" state, allowing data to be entered. HEN not only puts the counters in the hold mode but also keeps the load pin low which causes whatever is on Pins 3 through 6 of U1 through U3 to be transferred to Pin 14 through Pin 11 of their respective counter on each clock edge. So each uP cycle the address is transferred through, the counters to the horizontal memory map address inputs which selects the desired byte or nibble if the respective chip select, CS1 through CS4, is asserted.

The vertical section is composed of RAMs U10, U11 and U12, counters U4, U5 and U6, flip-flop U17, U18 and U19, buffers U23 and half of U22, Programmable Logic Array (PAL) U25 and various control gates.

The vertical section operates identically to the horizontal section with some slight deviation. When VEN is low the system clock (CPU) is used to transfer the CPU addresses through the vertical counters U4 through U6 to the vertical memory U10 through U12. This is because the normal clocking source for the vertical is 2H count which is extremely slow and would not latch the address correctly, and probably the 2H count would be disabled. The data transceivers are U23 and half of U22.

During the sync generator operation with VEN high, the data from the vertical is latched through U17 and U18. The signals on U18 are V front porch, V sync, V post and V trigger, all of which must be latched again by the trailing edge of 2H serrations in U19 to facilitate front porch during the Broadcast mode.

The PAL U25 combines the various signals to form composite sync, blanking, etc. All completed vertical rate pulses are routed to connector P2 for distribution.

The vertical counters are reset to initial conditions by the EOF command which is produced at the end of every two fields. Two fields are included in each count sequence to easily provide for interlaced systems in which two fields make an interlaced frame.

Gates U31A, U31B and U31C select the clock which will be used to control vertical rate operation. During normal sync generation, the VCLK signal is at 2H rate, transmitted through U31A to U31B, enabled by the HEN signal. When data is to be inserted into memory, the clock is taken from the CPU at 8 mHz; gate U31A is turned off by HEN and gate U31C is enabled by $\overline{\text{HEN}}$, allowing the CPU clock to pass through U31B. The horizontal enable signal can be used as memory load time is quite short and horizontal and vertical sections are disenabled simultaneously. The $\overline{\text{WE}}$ signal is used to enable buffers U22 and U23 when information is being written to the RAM. The data assignment is:

U10 - V Blanking, V Drive, V Window, End of Field.
U11 - V Front Porch, V Sync, V Post, V Trigger.
U12 - H Bar, H Crosshair, APL Gate, V Gate

NOR gates U20A and B serve as a comparator, sampling address lines BA-15 - BA-19. The resulting output of U20A is routed to PAL U24. If address commands are appropriate, logic as programmed in the PAL allows the $\overline{\text{SEL}}$, $\overline{\text{EPR1}}$, $\overline{\text{EPR2}}$ and R/$\overline{\text{W}}$ commands to be developed. Thus, bi-directional transceiver U28 may transfer data between card circuitry, enabled by the $\overline{\text{SEL}}$ signal. The direction of data transfer is dictated by the R/W signal.

Buffers U26 and U27 isolate data from the MBA PROGRAMMABLE SYNC bus for routing to both horizontal and vertical rate counters for writing data into the memories.

Programmed data is stored in EEPROMS U32 and U33. Data is obtained from buffers U26 and U27; the storage operation is controlled by flip-flop U30A. Two EEPROMs are used to obtain sufficient storage capacity for 68 raster formats. Each format is assigned an access number; 1 through 34 are stored in U32, U35 through U68, and U33. The EEPROMs require several commands for read and write operations:

1. The EWE (EEPROM Write Enable) command (to Pin 21 of the EEPROMs) generated by U30A must be at low level for the EEPROM to be written to; storage of a byte in one location requires 10 msec. Therefore to store one raster, time required is 2048 x 10 msec. While the EWE command is low, the address and data are internally latched and cannot change. When the EWE command returns to high level, the next storage command is received from the CPU SYNC GENERATOR card. EWE goes low, and the process is repeated. The EWE pulse is generated by U30A as commanded by the ESTB signal from Programmable Logic Array (PAL) U24; the ESTB is a combination of the R/$\overline{W}$ (Pin 3) and EPROM select (Pin 23) signals in the PAL.

2. The EOE (EEPROM Output Enable) command allows an EEPROM to be interrogated or read when a raster format is requested. The EOE command is developed by gate U38A, and is a combination of the "read" and EPROM select signals.

3. Which EEPROM will be read or written to is determined by the EPR1 and EPR2 signals developed by PAL U24, combination of address command A11 and the EPROM signal.

The Parallel Interface Timer (U29) contains a total of 32 registers which control various outputs. Pins D0-D7, A1-A5, DTACK, RESET, READ/$\overline{WRITE}$ and inputs; all others are outputs. All are controlled by the CPU SYNC GENERATOR card signals routed through buffers U27 (A1-A5) and U32 (D0-D7). Outputs include:

VEN . . . Vertical Enable, Pin 18
HEN . . . Horiozntal Enable, Pin 17
EPEN . . . EEPROM Enable, Pin 19
BOUNCE . . not used in this application

The pulses not used on this card are routed to connector P2 for distribution on the MBA PROGRAMMABLE SYNC circuit card. Outputs to J1 are for a printer interface through connector J1 which possibly could be used for test and debug of the system, not used in this application or for expansion of the system.

The V Blanking input at Pin 32 is used to develop the Bounce function, not used in this function.

The PIT signal on Pin 41 is used to select the appropriate EEPROM for storage or retrieval of data.

Sync format can be selected as any one of six modes, Broadcast, Industrial or Military as "standard" or "custom" controlled by the FC0, FC1 and FC2 signals routed to PAL U25.

U36 is an 8 bit shift register that generates a "data acknowledge" (DTACK) command to the CPU whenever anything on the board, except the PIT, is selected. The PIT generates its own DTACK. The DTACK is routed through open collector transistor Q5.

The CPU SYNC GENERATOR card (2190, Position 19) controls all operations previously described. Operations on this card operate from an 8 mHz dedicated system clock Y1 which is completely independent of the 20 mHz raster clock.

Microprocessor U6, MC68008, controls the entire system. It is supported by several other parts:

Memory U1, a permanently programmed EPROM, contains the operating program. It is interrogated by the microprocessor for operating instructions during programming, storage, recall, build, edit or search modes.

Static RAM U2, 8K x 8, receives and stores information transmitted from the microprocessor as operations are in process.

The bipolar PROM U13 decodes the entire memory map, selecting various components as commanded by the microprocessor through A12 - A19 address inputs:

$\overline{\text{BSEN}}$ - Buss Enable Not, enables data to be transmitted to the motherboard bus through buffer U7.

$\overline{\text{ACIA}}$ - controls when U15, which communicates with the front panel display and keyboard, may transmit or receive data.

$\overline{\text{RAM}}$ - selects RAM U2 for use by U6.

$\overline{\text{PROM}}$ - selects EEPROM U1 for use by U6.

The microprocessor (U6) is a 32 bit CPU but externally configures as an 8 bit device. It transfers 8 information bits at a time and has an address space of 1,000,000 bytes, designated as A0 through A19. The address codes select a specific location in the memory map being interrogated, and are uni-directional outputs only. The 8 bit data being read or written from that address location is designated D0 through D7. The data pins are bi-directional, serving as inputs or outputs, as designated by the $\overline{\text{READ/WRITE}}$ command from Pin 30 of U6.

The $\overline{\text{AS}}$ command from Pin 28 is the Address Strobe; when at a "low" state, the address outputs are valid (active).

The $\overline{DS}$ command from Pin 29 is the Data Strobe; when at a "low" state, the data in/outs are valid (active).

The signal designated E at Pin 38 of U6 is a synchronous clock to synchronize operation of peripheral components that operate at a slower speed. It is at 800 kHz rep rate, being the 8 mHz clock from Y1, submitted at U6 at Pin 34, divided by 10.

The $\overline{BDTACK}$ input at Pin 31 is routed directly to the motherboard bus at P1, Pin B without a buffer. It is the line connection to the HORIZONTAL SYNC GENERATOR and VERTICAL SYNC GENERATOR circuit cards which indicate when operations are complete.

The ERR (ERROR) command at Pin 40 detects errors which may occur on the bus and tells the CPU that there has been a system error. This will cause the "HELP I AM BROKE" display message to appear.

Pins 41 (BIRQ, an interrupt input) and Pins 33, 42 are not used. Pin 39, $\overline{VPA}$ (Valid Peripheral Address) is routed to J-K flip-flop U14B from U14A. It may be used to synchronize the E clock and produce yet a slower clock (VMA) which may be used with components on other cards that operate at low speed. The slow clock ($\overline{VMA}$) is sent to buffer U10 for distribution.

Various function codes, FO at Pin 43, F1 at Pin 44 and F3 at Pin 45, are mixed at gate U12. They can relate status of microprocessor operations; the signal is routed to buffer U11 for distribution, although it is not used in this application.

Special consideration is required when power is applied to the system. The microprocessor must be initialized when power is applied by forcing Pin 32 (HALT) to a low state. This is accomplished by U3, a type 555 timer that develops a 100 msec. pulse only when power is applied. This pulse is applied to Pin 36 of U6 through inverter U4C. The pulse also is routed through inverter U4B to develop the $\overline{BRESET}$ command for initializing various other components, including U15 and routing to the bus at P1, Pin W.

Gate U17D is used to invert the RAM command to form the $\overline{OE}$ signal. This Output Enable command is routed to RAM U2 to allow data to be taken from the RAM.

Shift register U16 is used to verify that the system is operating. The Data Strobe ($\overline{DS}$) signal is inverted by U8D and submitted to U16 at Pin 9. When this input goes "low", the shift register begins to cycle as commanded by the 8 mHz clock inupt at Pin 8. Several operations occur:

Pin 4 goes high at the second clock cycle (250 nsec.), routed to gate U17C and combined with the RAM signal. If RAM is selected, the BDTACK signal goes low signaling completion of activity.

Pin 6 goes high at the fourth clock cycle (500 nsec.), routed to gate U7B and combined with the PROM signal. If PROM is selected, the BDTACK signal goes low, signaling completion of activity.

Pin 13 goes high at the eighth clock cycle (1 usec.), routed to gate U17A, where output Pin 3 goes "low", generating the $\overline{\text{ERR}}$ (Error) signal. If there is not a response on the Data Strobe input in 1 usec., the "HELP I AM BROKE" message will be displayed, indicating that the system has attempted to use invalid data, an invalid address, etc.

Buffers U7-U11 are used to communicate from the CPU SYNC GENERATOR card to the rest of the system. While U7 is bi-directional to handle a two-way data communication, U8-U11 are uni-directional. Note that signal coding includes a B (Bus) prefix. This is merely to signify that the signal is located on the Bus side of the buffer rather than within the circuit card processing circuitry.

Circuit U15 is a Dual Universal Asynchronous Receiver-Transmitter (DUART) which is used to communicate with the keyboard and display on the front panel. This sub-system operates from its own clock, crystal Y2 at 3.6864 mHz, which is counted down within U15 to produce a baud rate of 1200 Hz. Basically the DUART consists of two serial ports plus input and output digital processing. The A side (RTSA Pin 29, CTSA Pin 7, RXDA Pin 31 and TXDA Pin 30) is used to write the display. The B side (RTSB Pin 12, CTSB Pin 4, TXDB Pin 10 and TXDB Pin 11) is routed to the keyboard/display assembly but is reserved for remote control/debug use in other applications. Display data transmission is by serial 8 bit word (TXDA Pin 30) usually in ASCI format but, when required, a special control character. The input (IP2 Pin 36, IP3 Pin 2, IP4 Pin 39 and IP5 Pin 38) and output (OP2 Pin 28, OP4 Pin 27, OP5 Pin 14, OP6 Pin 26, and OP7 Pin 15) are used to scan the keyboard, display, SAVE button, mode indicator lights, etc.

All of this communication is with the KEYBOARD INTERFACE (2194) circuit card by a 40 conductor ribbon cable to J1. As noted, the remote control port and associated circuitry (P1, J6, J7, U1, U2, C2 and C3) are not used in this application. The function of this circuit card is to scan the keyboard, display and other indicators.

The TXDA signal is routed from J1 directly to the display through J2, serial data to the display sub-assembly.

Lines RTSA (OP0), OP6 and OP7 are routed to decoder U3A where commands for the LED indicators are developed:

BUILD . . Pin 12 low
EDIT . . Pin 11 low
SEARCH . Pin 10 low
STORE . . Pin 9 low

Decoder U3B and multiplexor U4 scan the keypad. Microprocessor commands, processed through the DUART, cause Pins 4, 5, 6 and 7 of U3B to be "low" in sequential fashion, scanning the rows. Multiplexor U4 is operating at a faster rate; whenever a column is selected that is low, IP4 (Pin 7 of U4) also goes low. The specific line in "low" condition is decoded by outputs on Pin 2 (OP5) and Pin 14 (OP4).

The IP3 line is routed directly to the FORMAT STORE switch which causes the line to be grounded when the switch is pressed. However this command is ignored unless the microprocessor is requesting such action, as indicated by the SAVE LED indicator. The MBA PROGRAMMABLE SYNC circuit card (2193) is an assembly of connectors and interconnecting traces to route signals from one card to another. Signal distribution has been standardizd so that the CPU SYNC GENERATOR, HORIZONTAL SYNC GENERATOR and VERTICAL SYNC GENERATOR circuit cards can be inserted in any position without damage or malfunction. All connectors are 22 pin dual side, allowing 44 connections per connector. There are two connectors per card; P1 (facing front of unit) carries only internal computer signals. Connector designated P2 (facing rear of unit) carries various pulse signals which, eventually, are routed out of the sync generator assembly. Pin assignments are shown on layout drawing DL-2193 in the drawing section of this manual. Pull up resistors are provided for data lines that require them, in resistor networks RN1 through RN6. Connector J13 is used to provide power (+5v.) and ground to the KEYBOARD INTERFACE assembly.

A special connector is included in the MBA PROGRAMMABLE SYNC card for the uPROCESSOR INTERFACE card, which can be either 2196 (standard) or 4015 (optional). The uPROCESSOR INTERFACE card may be installed in this position only. No other type of card may be installed in this position. The uPROCESSOR INTERFACE card merely isolates, shapes and corrects polarity of signals to be presented to individual, open collector (optional load resistor) outputs. Octal buffers U1, U2 and U3 isolate output circuitry. Inverters are used where appropriate to change pulse polarities:

U4A to invert the H Drive signal.
U4B to invert the H Blanking signal.
U4C to invert the Blanking signal.
U4D to invert the 40H clock signal.
U4E to invert the V Blanking signal.
U4F to invert the V Drive signal.

Flip-flop U5A is used to develop a 20H rate pattern clock from the computer generated 40H pattern clock. Flip-flop U5B is used to count the V Bar Clock (which may be programmed or "standard" which is computer developed) from nominal 40H to 20H rate. Horizontal rate blanking is inserted into these signals at the clear (CIR) input.

All signals are routed to individual output stages, using discrete transistors on the 2196 uPROCESSOR INTERFACE circuit card and using IC inverters (7406) on the 4015 uPROCESSOR INTERFACE circuit card. In each case, an open collector output is provided with optional collector resistors installed as the particular application may demand.

Video and Pattern Generator Section

Circuit cards in this section contain circuitry to (a.) develop specific patterns from timing signals developed in the sync generator section, and (b.) translate signals and pulses into the format, level and impedance required for transmission of the instrument.

The video level sync generator signals from the programmable sync generator section (H Drive, V Drive, Blanking and Sync) are processed through the PULSE OUTPUT (2003, Position 11C) circuit card to properly drive coaxial cable at the required amplitude and impedance. Four identical circuits are used. The input is routed through bias network R1, R2 to saturating stage Q1. The collector waveform from Q1 is routed to push-pull output drivers Q2, Q3. Diodes CR1, CR2 between Q1 collector and load resistor R3 compensate for the base-to-emitter drop of the output drivers. Series resistors R4 and R5 provide a ground return path. The output is a.c. coupled through C1 to the output. Pulse amplitude must be controlled; control is obtained by the level of voltage directed to collector load R3, established by series regulator Q13, in turn controlled by potentiometer R25.

The TTL level output pulses are identified as H Trigger and V Trigger (as opposed to H Drive and V Drive for video level pulses). The V Trigger and H Trigger are variable in both position (phase) and width independently of the H Drive. Therefore the leading edge of the H Trigger can be positioned to lead, lag or be coincident with the leading edge of H Drive and the horizontal component of Blanking, as may be desired to locate information in the horizontal plane on a television display. Similarly, the V Trigger pulse can be located anywhere within the vertical raster time, as programmed, with width as programmed.

The TTL level pulses are processed for output drive on the TTL PULSE OUTPUT (2118, Position 12C) circuit card. This card contains six identical processing sections for the H Sync, V Sync, H Trigger, V Trigger, Blanking and Sync pulses. Each can be selected to be a positive or negative pulse. For instance, the H Sync pulse is routed into the card at Pin H to buffers Q5 and Z6C. From the buffer, the pulse is routed to control gate Z7A and also through inverter Z6B to control gate Z7B. The pulse which is to be used, as developed at R29, depends upon the control voltages at pins 2 and 5 of gates Z7A and Z7B. If Pin 2 is at high level and Pin 5 is low, gate Z7B is blocked, but Z7A is operating and the pulse passes through. Selecting Pin 5 high and Pin 2 low (by installing jumper U-V) will block Z7A and allow Z7B to be operational, developing a pulse of opposite polarity at R29. The pulse selected is routed to TTL driver Z8B for generation of the output, which is routed to the rear panel connector. Note that several options are available for the output circuit including 74128 (a TTL line driver), 7428 (a TTL regular buffer), or 7433 (a TTL buffer with open collector outputs). The 74128 line driver is supplied, unless otherwise specified.

Basic Video Signal Development

The video signals are developed on the TTL VIDEO (2155, Positions 3C, 4C and 5C) circuit cards which combine the various pattern elements, analog gray scale information, sync, and blanking, all of which are processed on the VIDEO CONTROL (4010) circuit card.

Gray scale is an analog video signal. It cannot be processed digitally as gray scale levels must be established at one point for all three output signals. The gray scale is developed at resistor R1 on the VIDEO CONTROL card with blanking inserted through Q1 to develop black level during both horizontal and vertical blanking intervals. The signal is routed to emitter follower Q2 which, with Q3, develops a "long-tailed pair" with Q3 acting as a black level clipper to insure a uniform black level exists for all variations of the Gray Scale pattern. The signal is then sent to emitter follower Q4, through filter R12, C4, R13 which conditions risetime to output emitter follower Q5. The low impedance output signal is passed through control R16 which allows the desired maximum white level to be established for different instrument configurations. The output from Pin Z is then routed to the level input of the video output cards.

The composite signal also requires blanking and sync for each channel. They are processed by similar fashion with the sync section used as an example. The sync signal is submitted through Pin A to gate Z1C which may be inhibited by grounding Pin B if a non-composite signal is desired. The signal is inverted through gate Z1B and passed to saturating stage Q8 which is biased to develop the signal between zero and -5v. It is necessary for the signal baseline to be at or near ground to avoid inserting a false d.c. component in the composite video. This signal is then routed to distribution emitter follower Q9 which has drive capability to send a full level signal to each of the three TTL VIDEO circuit cards. Gate Z1D, Z1A, saturating stage Q6, and emitter follower Q7 perform the identical function for the blanking signal.

The TTL VIDEO circuit card processes all pattern information into the output video signal. Pattern signals are coupled into the card through one of four routes. Fast rise signals are emitter coupled at a common junction of Q5, R15 through connector Pin W. Emitter coupling allows the fastest risetime, as it is at very low impedance. This is especially important for the Resolution function. Patterns which do not involve such fast risetimes may be coupled through a saturating transistor stage, Q9 in conventional logic fashion, where polarity inversion is desired (Pin P). Patterns which do not require inversion, such as Color Bars, may be routed directly to collector resistor R19 through Pin Y.

RGB color signals require different video information for each output video channel. Signals from the CLOCKED COLOR BAR circuit card are inserted through Pin Y to the collector of Q8 for processing. Inverting and non-inverting digital inputs are routed to emitter follower Q5. The emitter-coupled inputs (Pin W) are connected to the output of this stage at the junction of R15 and Q5 emitter, where all video elements are brought to a common point, but inverted. This low impedance point drives saturating stage Q4, which establishes the proper signal polarity at fast risetimes. The Gray Scale input circuit includes an emitter follower Q3, which drives a resistive bias network. The bias adjusted by R8 is used to adjust Gray Scale signal black level as close as possible to the black level of the digital signal which is formed at Q4.

The digital signal goes to PNP emitter follower Q2, the incoming Gray Scale to Q1. The emitters are coupled together to R11. With the PNP transistor pair, the emitter with lower voltage controls, back-biasing the other one. Therefore this pair operates as a level control, clipping off the digital video signal as directed by the Gray Scale input. In this way the video level is controlled without sacrifice in digital signal rise and fall times. The signal is routed to emitter follower Q10 for distribution to the TTL and composite video output circuits.

Video for TTL output is routed through d.c. bias diodes CR4, CR5 and CR6 and bias network R64, R66 to PNP emitter follower Q20. This feeds the output push-pull driver Q18, Q19. Network R57, R59 and R60 develops 75 ohm source impedance to properly feed a coaxial cable.

The video signal is routed to an emitter follower network which mixes the blanking and sync signals to form the composite video.

The blanking and sync signals are processed on the VIDEO CONTROL card for use on the TTL VIDEO cards for development of a composite video output signal.

The sync signal is processed by Q12 and is fed into the network by R36. All three components of the composite signal are formed at R37.

The composite signal is routed to two emitter followers, Q13 and Q15, which filter the signal slightly to remove spikes from the very fast rise and fall times (C9). Circuitry d.c. levels have been chosen to generate the blanking level (blacker-than-black) at near ground potential. Component tolerances make this level difficult to control absolutely, so adjustment of R42 is made to inject sufficient bias current to bring blanking level in the output signal to ground potential, and to compensate for d.c. shifts encountered in the output driver. The push-pull complimentary pair driver, Q16 and Q17, is fed by PNP emitter follower Q15, which also includes diodes CR1 and CR2 to compensate for base-to-emitter voltage drops in the driver transistors. Source impedance is determined by the built-out resistor network R52, R53 and R55.

Function Select

The various patterns are selected by switching control points to ground on the appropriate circuit cards. Only the cards necessary to produce a certain pattern are in operation at one time, therefore assuring no interference from circuitry within the instrument operating at different times.

Flat Field

Often it is desired to have the Flat Field function at some level other than 100% white; circuitry for this is on the GRAY SCALE (4000, Position 4B) circuit card. Flat Field level is considered an analog function since it must be processed through video level controls at the output video circuitry.

Selection of Flat Field causes Pin C of the GRAY SCALE card to be grounded. Inverter Z9B output goes high, causing the output of inverter Z9C to go low, conducting, thus connecting level control R18 to be effective. The Flat Field level desired is adjusted at R18, lowering the gray scale bus (Pin A) as required.

If 100% white level is desired for the Flat Field function, remove resistor R23 from the GRAY SCALE circuit card. Therefore, control R18 can never cause variation to gray scale bus level.

Bars and Dots

The Bars and Dots patterns are developed by the CLOCKED BAR/DOT circuit card (4003, Position 8B) operating as commanded by horizontal and vertical rate information from the programmable sync generator section. V bars are developed from the 20H clock which is submitted through Pin S to isolating gate Z2C. Clocked pulses are routed through emitter follower Q3 to charge capacitor C4. The negative transition is passed to the base of Q1 which becomes non-conductive. Charging network R11, Q2, C4 is a constant-current generator which determines the amount of time taken until C4 charges to the point that transistor Q1 becomes conductive. When that occurs, the collector of Q1 goes negative terminating the V bar pulse. The rate of charge is determined by the bias at the base of Q2, the control voltage either developed from R8 or submitted at Pin B passed through attenuator network R10, R14 which determines the range of control. The positive pulse from the collector Q1 is routed through resistor network R12, R15 to the base of transistor Q4 where the inverted (negative) V bar pulse is developed.

H bar elements may be submitted at Pin F but, in this instrument, are developed in the programmable sync generator, and therefore are submitted at Pin C. The H bar elements from the sync generator are programmed into increments, meaning that due to either the H BAR POS (Parameter No. 25) or the H BAR SPC (Parameter No. 22), an H bar could be commanded to begin in the middle of a scan line. This is not desirable so an interlock network is used to insure that horizontal bars always cover a complete scan line. When a positive H bar gate occurs at Pin C, gate Z4A is enabled allowing the horizontal blanking pulse to pass to "set" bistable Z4B, Z4D. The H bar gate is always two half-lines long insuring that only one H blanking pulse is submitted to the bistable. When the H bar gate terminates, gate Z4C is enabled submitting the horizontal blanking pulse to Z4B, forcing the bistable to revert to its original state. This state persists until the next H bar gate signal occurs. Control logic is included on this circuit card to combine the vertical and horizontal rate elements into the bar, dot, H bar or V bar patterns as desired. To select the Bars function, Pin W is grounded inhibiting gate Z1A. Therefore, the H bar element from bistable Z4B, Z4D inverted by Z3F, is allowed to pass through gate Z1B causing a "low" level to be developed at the collector of Q4. When horizontal bars are not present, Z1B is inhibited by the low state at Pin 6. During these times, the V bar pulse from Q4 is present. Therefore, if Pin V is grounded and Z1D does not prevent signal development, the pattern is submitted to Pin 9 of Z1C and inverted to the output at Pin U.

If Dots are desired, Pin H is grounded. Therefore, the output of inverter Z3E goes high allowing H bar elements to be passed through gate Z2A inhibiting the 20H clock from passing through gate Z2C except on lines in which dots are desired. That is, dots are developed by generating V bars only on selected lines. The H bar gate also is passed through Z2B and Z2D causing the collector of Q1 to be at a "low" state except on the lines in which dots are developed.

All of these signals are combined at the collector of Q4 and submitted to gate Z1C for development of the output.

Gray Scale

Gray Scale in this instrument is presented in two ways - a separate function and as a part of the Video test signal. In each case a linear, ascending ten level (eight shades of gray plus black and white) Gray Scale is used. The format is selected by control circuitry on the GRAY SCALE SELECT (4007, Position 5B) card the gray scale steps are developed on the GRAY SCALE (4000, Position 4B) card which also contains circuits to develop other analog signal levels, including Flat Field (usually at 50% gray) and the gray level presented between Resolution bursts (usually at 50% gray level also).

Gray scale step development is controlled by a ring counter composed of J-K flip-flops Z1, Z2, Z6, Z7 and Z8. The rate and time for ring counter operation is determined by clock input at Pin N and the gray scale gate input pulse at Pin W which allows the count sequence to start.

When the gray scale circuitry is to be inactive, all ring counter elements have the "clear" input at a low state. The control is submitted from Pin K to inverter Z5A, thus the control input is at a high level to inhibit gray scale development.

When the gray scale is to be enabled, the control input goes to the low state, releasing the "clear" previously imposed on ring counter elements. The positive transition at output of gate Z5A also allows bistable Z5B, Z5C to operate when commanded. Even though clock pulses may be present, nothing can happen with circuitry in this state.

Flip-flop Z1B initializes stage Z1A which develops prime pulses. Note that, in some applications, Z1 could be removed and prime pulses can be submitted through Pins U and W from an external source. When the Prime A and Prime B pulses occur, several things take place. Prime A is a positive pulse, Prime B negative.

Black level is the first Gray Scale step. It may be equal in width to other steps, or may be required as a wide margin. Jumpers are provided to select the type of black desired. If a wide margin is desired, jumper A-C is installed. Output of bistable Z5B, Z5C is low, the output of gate Z5D is high, causing inverters Z3B and Z3E to have a "low" output state, generating black video level. The Prime B pulse forces the bistable to change state, allowing the black margin to be terminated when the Prime B pulse ends.

If only a black step is desired, jumper A-B is installed, causing black level to be developed by Z3B and Z3E while the Prime A pulse occurs. Jumper A-D allows external control of black level if so desired, as when various Gray Scale modes are to be used.

When the prime pulses occur from Z1A, all of the type D flip-flops are Preset, and simultaneously change state at the next clock pulse edge. Thus, all control inverters, Z3A, Z3F and Z4A-F saturate, connecting all step level controls (R1 through R8) to ground.

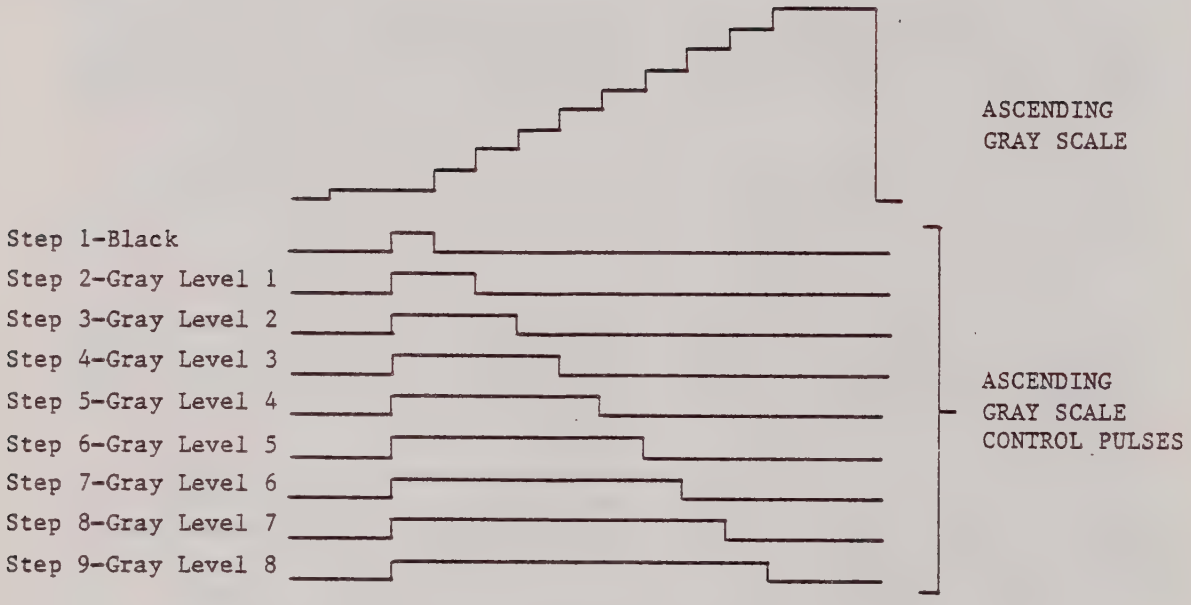

Figure 24 - Gray Scale Waveform Logic

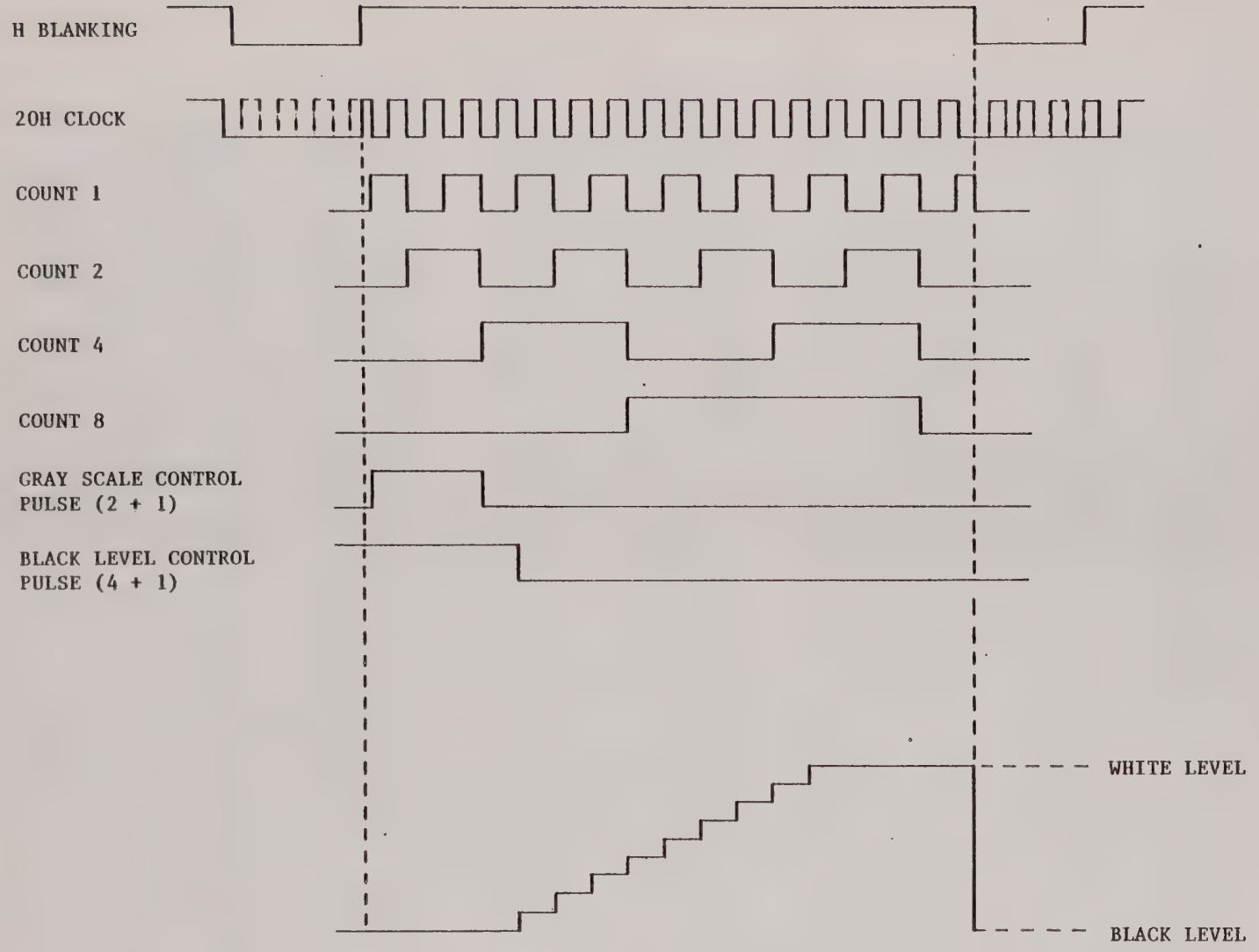

Figure 25 - Gray Scale Position Logic

At the next clock cycle, flip-flop Z6A changes state; inverter Z4A becomes non-conductive and control R1 is disconnected. The output of Z6A is connected to the "D" input of Z6B, therefore Z6B can change state at the succeeding clock pulse cycle. This sequence of operation develops a stepping type of control as shown in Figure 24 (page 172), sequentially disconnecting each step level control. Of course, control settings determine the step characteristic, usually linear.

The GRAY SCALE card also contains circuits to develop the Flat Field, gray level between Resolution bursts, and the "whiter-than-black" segment of the Black Reference segment of the Video and Combination test patterns. These will be discussed in the appropriate function text.

As noted, the rate at which the Gray Scale is developed is determined by the GRAY SCALE SELECT card. The separate gray scale is placed in the middle of each horizontal line, per Figure 24 (page 172), and is developed from a 20H rate clock generated by the sync generator section, whereas the gray scale portion of the Video test pattern is shorter (see page 59) and therefore developed from a 40H rate clock. This selection is made by gates Z7C and Z6D, with the output clock processed and inverted by Z6C for routing to the GRAY SCALE circuit card.

Similarly the gray scale control pulse is selected by gate Z7D, Z6A and inverter Z4C. The gray scale control pulse for the Video function is developed by bistable Z4A - Z4D on the VIDEO CLOCK (4001, Position 6B) card, submitted to gate Z7D on the GRAY SCALE SELECT card. The control pulse for the separate gray scale is developed by bistable Z5A, Z5B on this card also.

When the black level occurs, it is established by gates Z7A, Z6B and inverter Z4F. For the Video pattern, the Prime A signal from the VIDEO CLOCK card ring counter (Pin W) is routed through Pin Z to gate Z7A. For the separate Gray Scale pattern, a black margin is used from the start of an active line (left edge) to the first gray level above black, with the control gate developed by bistable Z5C, Z5D.

Generation of control gates for the individual Gray Scale function is controlled by binary counters Z1, Z2. The 20H clock, processed through inverter Z4E is routed to the clock input of Z2A. When Gray Scale is selected, the J input is high, allowing Z1A, Z1B, Z2A, Z2B to operate as a four section binary counter. Outputs are summed by gates Z3A and Z3B to develop the desired control pulse for latches Z5A, Z5B and Z5C, Z5D.

The +H gate signal, which can be either H drive or H blanking, is inverted by Z4D; the negative pulse causes both latches to change state. Thus the latch outputs command black level to start (Z5C, Z5D) and gray scale to be inhibited (Z5A, Z5B), when the desired count is reached by the binary counter gates as shown in Figure 25 (page 173). Note that latch Z5A, Z5B locks out further operation by feeding its output to gate Z3B (Pin 4) until the latch is reset by H blanking. This precludes a false turnoff of the gray scale by the binary counter subsequent counts. At the end of the line, the binary counter is cleared to an initial state by the H gate input; latches Z5A, Z5B and Z5C, Z5D also are reset so that the cycle may be reinitiated for the next horizontal scan line.

V Stripe and Window

These patterns are related, derived from timing pulses as programmed, in the sync generator section. The V Stripe is a presentation of a white segment in each scanning line of the raster. Position and width of the segment is programmed by H WIN START (Parameter No. 23) and H WIN STOP (Parameter No. 24). The Window pattern is the V Stripe which has been enabled by a V window gate, also programmed in position and height by V WIN START (Parameter No. 27) and V WIN STOP (Parameter No. 28).

The H window gate is routed from the uP INTERFACE circuit card through Pin X of the PATTERN LOGIC card (4006, Position 9B) to gate Z3C. If V Stripe is selected, Pin W is grounded, inhibiting gate Z3B from transmitting the V window gate. The output of Z3B is "high" allowing the H window gate to be conducted to output gate Z4D. Gate Z4C is inhibited by output of Z5D and gate Z3D is inhibited by V Stripe selection.

If the Window pattern is selected, the V window gate input at Pin D is utilized. Pin Y controls pattern development, being grounded to select Window. The control gate is developed in the sync generator section, programmed for position (starting point) and width (height of the V window gate) in half line increments. A half line increment of pattern is not desirable, so the control gate is latched to blanking by bistable Z1C, Z1D. At the start of the vertical rate field, the gate input at Pin D is at "low" level. Therefore gate Z1A is blocked, but gate Z1B may conduct due to inverter Z6B. The blanking signal, processed through inverter Z6C, is transmitted through gate Z1B to set bistable Z1D.

The "low" output of the bistable is routed to gate Z3A, which is inhibited. Therefore the output of gate Z3B is "low", inhibiting gate Z3C; the "high" output of gates Z3C and Z3D causes the output of Z4D to the pattern bus to be "low", generating video black level.

When the gate occurs, as programmed by V WIN START (Parameter No. 27), the polarity at Pin D goes "high". Therefore gate Z1B is inhibited and Z1A is enabled. Thus the blanking signal is routed to Z1C, causing the binary Z1C, Z1D to change state. The output is now "high" causing the output of Z3A to be low, the output of Z3B is to be "high". Therefore the +H window gate is allowed to pass through Z3C to output gate Z4D.

At the end of the gate, programmed by V WIN STOP (Parameter No. 28), gate Z1A is inhibited, Z1B is enabled, and the binary reverts to original state once again forcing gate Z4D to develop video black level as described above.

Resolution

Resolution is used as an individual function and also as a component of the Video test pattern. The same circuitry is used for both patterns. Basically the Resolution pattern is alternate black and white video developed by the output of an astable multivibrator; one RESOLUTION circuit card (4013 in Position 7C) is provided for all burst rates, with control voltage varied to produce the desired repetition rates.

Transistors Q9, Q17 are the output stages of an astable multivibrator which is phase-locked to the horizontal. Circuitry is extensively decoupled and employs low impedances to provide the fastest possible repetition rate.

In the "off" state, as during blanking or when this function is not being used, control circuitry develops a negative output at emitter follower Q6 causing diode CR3 to conduct. This clamps the astable to an inactive state with transistor Q9 non-conductive due to its low base voltage. The base of Q17 is at high level due to the constant current charge of capacitor C3; Q7 is saturated, providing a "low" output through emitter follower Q18.

When the emitter of Q6 goes high, diode CR3 becomes non-conductive. Capacitor C4 charges, in linear fashion, at a rate determined by constant current source Q15-R38, the charge rate controlled by the voltage bias at the base of Q15. Capacitor C4 charges until its voltage is raised to the point that Q9 conducts; Q14 provides a low impedance feed for the Q9 base. Diode CR2 limits the charge maximum level. At this point Q9 conducts, the negative transition routed through emitter follower Q10 to capacitor C3, where the same charging sequence occurs until Q17 conducts. The negative transition from the collector of Q17 is routed through emitter follower Q16 through C4, Q14 to the base of Q9 which then becomes non-conductive; its collector goes "high". Capacitor C4 once again becomes charging, repeating the cycle until clamp diode CR3 once again conducts.

Components C3, C4, R34 and R38 are selected to provide the rep rate control range desired. The exact rep rate is then determined by the voltage applied to the base of Q13, Q14. This voltage is set by controls R2, R5, R8, R11 and R14 which are switched into the circuit by saturation of Q1-Q5 by applying positive voltage to the appropriate control input, Pins V, W, X, Y or Z. Control logic circuitry is on the RESOLUTION CONTROL circuit card (4002, Position 7B).

On-off control signals for the astable multivibrator are processed by stages Q7 and Q8. Signal development is controlled by the waveform submitted to Pin P from the RESOLUTION CONTROL card, directed through R24 to Q8. In turn, load resistor R19 will control the output level of emitter follower Q6 through bias network R20, R21. When Q8 saturates due to a "high" condition of the input duty cycle signal, a low level is developed at the emitter of Q6, clamping the astable. When Q8 is biased "off", the astable is operative. Blanking is submitted to Q7 to clamp the astable "off" during horizontal and vertical blanking.

If Resolution is selected as a single function, Pin Y of the RESOLUTION CONTROL card is grounded. The output of gate Z7B goes high, allowing the 20H clock to pass through gate Z6D to control RESOLUTION card astable to operate in bursts. The astable rep rate is selected by which gate Z5A, Z5B, Z5C, Z5D or Z6A is activated by grounding Pins S, P, M, J or F respectively. Ring counter Z1, Z2, Z3 is not active in this case.

When the Video function is activated, the ring counter controls resolution generation. Bistable Z6B, Z6C generates the control gate to turn the RESOLUTION circuit card astable on, through gates Z7B and Z6D. The rep rate is established in proper multiburst sequence by ring counter outputs to control gates Z5A, Z5B, Z5C, Z5D and Z6A.

Usually a 50% gray level is desired between Resolution bursts. Adjustment for this is on the GRAY SCALE circuit card (4000, R17) as controlled by gate Z7A and inverter Z4D on the RESOLUTION CONTROL card. The 20H clock is submitted to gate Z7A to develop gray level whenever the resolution astable is gated "off", controlled by the output of gate Z7B.

Color Bars

This function is developed by the CLOCKED COLOR BAR circuit card (4008, Position 6C). The Color Bars pattern is developed as a series of gated levels from each of the red, green and blue video outputs. The basic pattern is generated by a counter operating from a 20H clock developed in the sync generator section.

The clock is submitted through inverter Z2C to the clock input of J-K flip-flop Z3A.

Binary counters Z3 and Z4 divide the clock pulses into 4H rate for the blue color signal (Z4B), 2H rate for the red color signal (Z3B), and H rate for the green color signal (Z4A). The 8H output of Z3A is not used. The signals are routed to open collector output inverters Z1A, Z2B and Z1C for transmission to video output cards.

The counters must be reset to initial condition before the start of each horizontal line. Therefore the +H blanking signal is routed into the card through inverter Z2B. The processed pulse is fed to the clear input of all J-K flip-flops.

Selection of pattern is provided by inverter Z2A and gate Z1D. If Color Bars is not being used, Pin 12 of gate Z1D and Pin 1 of inverter Z2A are high, dictating a low level output from these stages. Therefore the J-K flip-flops are all at the clear state and are inoperative. The low output of gate Z1D also inhibits output gates Z1A, Z1B and Z1C, forcing the outputs to a high (inactive) state.

An optional circuit is used for processing of the blanking signal, submitted to the digital pattern bus in some instruments. Resistor R3 serves as a collector load for all patterns, such as Bars, Dots and Window which are routed onto the common bus. Blanking is submitted to saturating state Q5 which develops black level on the pattern bus during blanking.

RGB color systems require that the Resolution and Character signals, emitter coupled for fastest possible speed, be split three ways. Emitter followers Q1, Q2, Q3 and Q4 provide this distribution to the three separate video output cards.

Video

The Video test pattern is a combination of the Resolution and Gray Scale functions plus a Black Reference segment. It operates from a 40H rate clock as shown in Figure 26 (page 180). Pattern timing functions are controlled by the VIDEO CLOCK (4001) circuit card. The sequence of pattern element generation is controlled by a ring counter which is distributed among the VIDEO CLOCK, RESOLUTION CONTROL and GRAY SCALE circuit cards.

Resolution is presented as a multiburst, five steps, with bursts separated by a 50% gray level and preceded by a white/black reference segment which is controlled by ring counter Z9, Z10 on the VIDEO CLOCK card. The 40H clock is routed through inverter Z7E if polarity must be inverted, using jumper A-B; jumper A-C is used for a non-inverted 40H clock. The selected clock goes to inverter Z7B and from there to flip-flop Z9A where it is divided by two to a 20H clock which is routed to Pins H and N for use as desired elsewhere. The 40H clock is output at Pin Z for use elsewhere also. Resolution segments are developed from the 20H clock as shown in Figure 26 (page 180).

The output of Z9A is fed to the clock input of Z10A to initiate ring counter operation. Ring counter flip-flop Z9B counts a left margin at black level until the Reference (100% contrast) pulse occurs as commanded by the output of Z10B which is fed to gate Z8D.

Bistable Z4B, Z4C develops the black level left margin, being set by the H blanking pulse, causing inverter Z6A output to saturate, generating black level on the pattern bus, Pin R. Gate Z8D is thus allowed to conduct the 20H clock pulse through to inverters Z6E and Z6B, placing one cycle of the clock onto the pattern bus to serve as the white/black reference pulse.

The outputs of Z10B are routed out of the VIDEO CLOCK card, Pins K and L, to the RESOLUTION CONTROL card which, in turn, controls generation of the multiburst sequence generated on the RESOLUTION card. Ring counter outputs of the ring counter on the RESOLUTION CONTROL card are routed into the VIDEO CLOCK card, Pins X and Y, to control generation of the Black Reference segment. The last ring counter segment of the RESOLUTION CONTROL card develops a white segment which separates the Resolution and Black Reference segments.

A phase change is generated by Z1A by using the opposite polarity of 20H clock than is used in the Resolution section of the ring counter. Output of Z1A is routed to gate Z3A, where it is mixed with the 20H clock. Output of Z3A then causes bistable Z3C, Z3D to change state; the output of Z3C, Z3D is routed out of the card (Pin A) to the Whiter-than-Black control on the GRAY SCALE circuit card (4000, R19). This control remains energized through the black segment, when bistable Z3C, Z3D is reset by the output of Z1B.

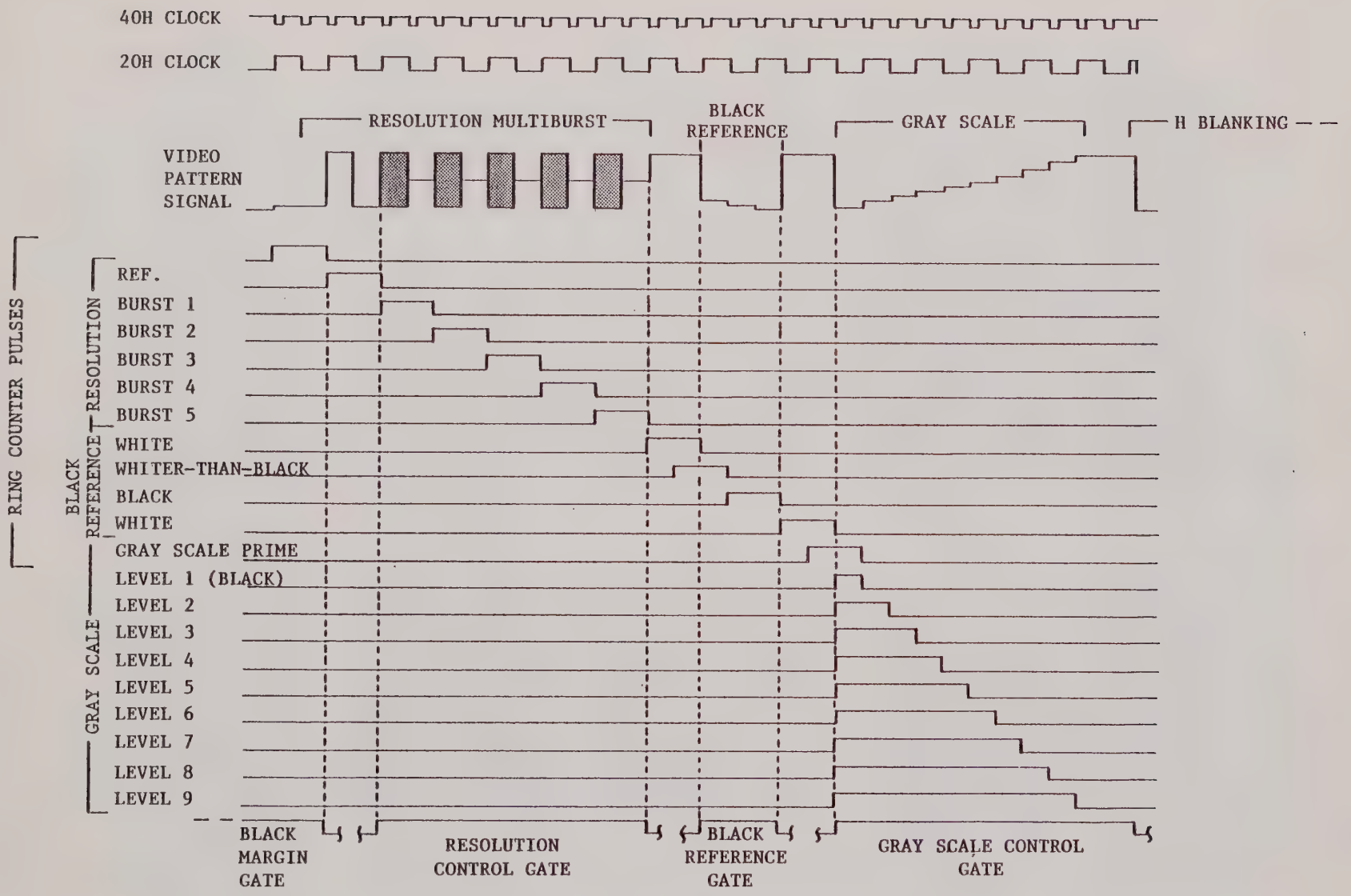

Figure 26 - Video Pattern Logic

The output of Z2B is routed to inverters Z5C and Z5D which develop black level on both the gray scale bus and digital pattern bus respectively for the black and blacker-than-black segments. The blacker-than-black segment is merely black level with a step inserted into the blanking signal to develop a reference level "below black" on the composite video signal. The black control pulse is used to open gate Z3B to pass one-half cycle of the 20H clock which then is mixed into the blanking signal at Z8B. The conditioned blanking signal is then routed to Pin C through two isolating inverter/buffers for routing to the TTL VIDEO circuit cards.

Ring counter segment Z1B develops a white segment to separate the Black Reference and Gray Scale functions. Segment Z2A causes bistable Z4A, Z4D to change state, generating a gate to control development of the Gray Scale. The bistable is reset by the H blanking pulse which occurs at the end of the active line. The output of Z4A, Z4D is routed to the GRAY SCALE SELECT (4007) card for control of gray scale generation.

All circuit elements are "cleared" to original condition at the end of each active horizontal line by H blanking as processed through inverter Z7A, gate Z8C and inverter Z7C. Inverter Z5B is used to inhibit the output of bistable Z3C, Z3D when the Video pattern is not being used.

Gate Z8A and inverters Z7D, Z6D and Z6C are used to develop the Reference Resolution pattern, derived from the 20H clock developed by counter Z9A.

Combination

The Combination pattern is a composite of Color Bars at top and bottom of the display with the Video test pattern inserted in a strip across the display center. Position and height of the strip is controlled by programming the APL function (Parameters 32 and 33) through the keyboard.

Circuitry for control of this pattern is on the PATTERN LOGIC (4006, Position 9B) circuit card. The APL control gate is developed in the sync generator section, programmed for position (starting point) and width (height of the Video pattern band) in half line increments. A half line increment of pattern is not desirable, so the APL control gate is latched to blanking by bistable Ƶ2C, Ƶ2D. At the start of the vertical rate field, APL gate input at Pin C is at "low" level. Therefore gate Ƶ2A is blocked, but gate Ƶ2B may conduct due to inverter Ƶ6F. The blanking signal, processed through inverter Ƶ6C, is transmitted through gate Ƶ2B to set bistable Ƶ2D.

The "low" output of the bistable is routed through inverter Ƶ6E to gate Ƶ4A. If the Combination pattern is selected, by grounding Pin R, the output of Ƶ5C is "high", allowing Ƶ4A to conduct. The "low" output at Pin P allows Color Bars to be developed. The output of the binary is also routed to gate Ƶ4B which is also enabled by Ƶ5C. However, the "low" binary output causes the output of Ƶ4B to be "high"; the Video pattern is not enabled.

When the APL gate occurs, as programmed by APL START (Parameter No. 32), the polarity at Pin C goes "high". Therefore gate Ƶ2B is inhibited and Ƶ2A is enabled. Thus the blankng signal is routed to Ƶ2C, causing the binary Ƶ2C, Ƶ2D to change state. The output is now "high", inhibiting Ƶ4A but enabling Ƶ4B, turning off the Color Bars and turning the Video pattern on by generating a "low" level at Pin N.

At the end of the APL gate, programmed by APL STOP (Parameter No. 33), gate Ƶ2A is inhibited, Ƶ2B is enabled, the binary reverts to original state, Video is turned off and Color Bars are developed once again. If the Combination pattern is not selected, Pin R is "high", the output of inverter Ƶ5C is "low" and both gates Ƶ4A and Ƶ4B are inhibited; neither Color Bars nor Video are enabled.

Video and Color Bars may be selected individually. To select Color Bars, Pin U is grounded. The control signal is inverted by Ƶ5E, causing the output of Ƶ5B to go "low" causing Color Bars to be developed. Similarly, selection of Video takes Pin V "low", output of inverter Ƶ5F "high", and Ƶ5A "low", therefore causing the Video pattern to be developed.

The clock for Character generation is taken from a RESOLUTION circuit card (4013 in Position 9C). See the Resolution section for description of card operation in the Continuous mode. The clock determines how many characters will be displayed across the screen.

The Character is developed on the CHARACTER card (4014, Position 8C). This card contains logic to properly interrogate a PROM (Programmable Read Only Memory) Z1, to develop the character, a block "C" with "x" superimposed as shown in Figures 21 and 22 (page 63). The character is of a 5 x 7 dot matrix in a 10 x 10 pixel area, giving five spaces horizontally and three spaces vertically to separate adjacent characters.

The +V gate input is inverted through Z5C and is used to clear the row counter. This is to synchronize the Character vertically. The +blanking input at Pin Z is used to synchronize the dot counter to the row counter and also synchronize it to the beginning of the horizontal line. This input is tied to the clear input of the dot counter. The +H gate input at Pin X is used solely to initialize the shift register at the beginning of the horizontal line; this is to exclude the possibility of a partial character remaining in the shift register during blanking and carried to the next row.

Beginning from the initial point, the clock is applied to Z4A, a high speed Schmitt trigger buffer, and inverted. The clock is then distributed to three sections, the dot counter Z3, shift register Z6 and 50%/100% delay section.

The dot counter sends out a "load" pulse (two clock periods wide) to load the character code from PROM Z1 into the shift register. The shift register shifts right one position on the leading edge of the dot clock. As each column of the character is shifted out it is inverted by Z5 and routed to the output through emitter follower Q1.

When the next horizontal pulse (blanking) is received the row counter is increased by one and the dot counter and shift register are again loaded. This continues until the last line of the field is encountered and the sequence starts again with initial conditions.

The code generator is the only section that remains and is purely passive. Z1 is a high speed bipolar PROM with 25 to 30 nsec. access time. It has a 38 x 8 bit organization. The row counter outputs (QA, QB, QC and QD) are tied to ADa, ADb, ADc and ADd respectively, the low order address lines of the PROM. Provision is included for ADe to access a second character. Normally ADe is tied to ground or low state. When ADe is pulled low the lower 16 words of the Cx are addressed and when high, the upper 16 words of the secondary character are addressed. The normal Cx character resides in the lower section of the code generator while the secondary character, if and as specified by the customer, is in the upper addressed section.

Character pixels from the shift register Z6 are routed to the type D flip-flop Z7 where they are latched to the trailing edge of the clock as inverted by gate Z10C. The output of Z7 is routed to gate Z10B where selection of 50% or 100% duty cycle pixels in the character is made. If jumper A-B is installed, the clock from Z10C inhibits gate Z10B for each clock half cycle. If jumper B-Y is installed, the control gate input is high and therefore effective, allowing 100% pixels to pass through the gate.

Exclusive OR gate Z9C provides polarity control. The character from flip-flop Z7 is of "white" polarity, inverted by Z10B. Therefore gate Z9C output is low (non-inverted) if control input at Pin 10 is low. The control is processed by isolating gates Z9D and Z5E; therefore jumper W-X is installed to develop the desired polarity. If jumper W-X is removed, the input to Z5E is high, output low causing output of Z9D to be high and Z9C to invert the character signal. The input bias to Z5E, R6 is routed to output Pin E so that remote control of polarity can be provided.

On-off control of the Character function is provided by gate Z5F. If the control at Pin T is high, inverter Z5F output is low. This forces Z2 and Z3 to the "reset" condition as they are set during blanking. Also the control signal, mixed with blanking during normal operation by Z5B, is used to inhibit gate Z10D, blocking the signal and forcing the output to a low state, the desired non-operating condition. Selecting the Character function grounds Pin T, causing the control bus to go high and therefore inactive; the Character is then developed.

The output is processed through gates Z10A and Z4C to output emitter follower Q1 for distribution.

SCHEMATIC AND LAYOUT DRAWING INDEX

S-3211 Overall Function Diagram - Model 2501

Programmable Sync Generator Section

S-3202 Function Diagram - Programmable Sync Generator Section
PL-2196 uProcessor Interface (Group 1)
DL-2196 uProcessor Interface (Group 1)
DS-2196 uProcessor Interface
PL-4015 uProcessor Interface (optional)
DL-4015 uProcessor Interface (optional)
DS-4015 uProcessor Interface (optional)
PL-2192 Vertical Sync Generator
DL-2192 Vertical Sync Generator
DS-2192 Vertical Sync Generator
PL-2195 Horizontal Sync Generator
DL-2195 Horizontal Sync Generator
DS-2195 Horizontal Sync Generator
PL-2221 H/V MPU Controlled Sync Generator (alternate)*
DL-2221 H/V MPU Controlled Sync Generator (alternate)*
DS-2221 H/V MPU Controlled Sync Generator (alternate)*
PL-2190 CPU Sync Generator
DL-2190 CPU Sync Generator
DS-2190 CPU Sync Generator
PL-2201 Power Interface
DL-2201 Power Interface
PL-2193 MBA Programmable Sync
DL-2193 MBA Programmable Sync

*H/V MPU Controlled Sync Generator circuit card may be used in place of both the Vertical Sync Generator (2192) and Horizontal Sync Generator (2195) circuit cards.

Pattern Generator Section

S-3203 Function Diagram - Pattern Generator Section
PL-4010 Video Control (Group 1)
L-4010 Video Control (Group 1)
S-4010 Video Control
PL-4000 Gray Scale (Group 2)
L-4000 Gray Scale (Group 2)
S-4000 Gray Scale
PL-4007 Gray Scale Select (Group 0)
L-4007 Gray Scale Select (Group 0)
S-4007 Gray Scale Select
PL-4001 Video Clock (Group 0)
L-4001 Video Clock (Group 0)
S-4001 Video Clock

Pattern Generator Section (cont.)

PL-4002	Resolution Control (Group 0)
L-4002	Resolution Control (Group 0)
S-4002	Resolution Control
PL-4003	Clocked Bar/Dot (Group 2)
L-4003	Clocked Bar/Dot (Group 2)
S-4003	Clocked Bar/Dot
PL-4006	Pattern Logic (Group 1)
L-4006	Pattern Logic (Group 1)
S-4006	Pattern Logic
PL-2110	Power Regulator (Group 1)
L-2110	Power Regulator (Group 1)
S-2110	Power Regulator
PL-2155	TTL Video (Groups 7, 8)
L-2155	TTL Video (Groups 7, 8)
S-2155	TTL Video
PL-4008	Clocked Color Bar (Group 1)
L-4008	Clocked Color Bar (Group 1)
S-4008	Clocked Color Bar
PL-4013	Resolution (Groups 1, 2)
L-4013	Resolution (Groups 1, 2)
S-4013	Resolution
PL-4014	Character (Group 0)
L-4014	Character (Group 0)
S-4014	Character
PL-2003	Pulse Output (Group 1)
L-2003	Pulse Output (Group 1)
S-2003	Pulse Output
PL-2118	TTL Pulse Output (Group 5)
L-2118	TTL Pulse Output (Group 5)
S-2118	TTL Pulse Output

Keyboard Assembly

S-3210	Function Diagram - Keyboard/Display Interface
PL-2194	Keyboard Interface
DL-2194	Keyboard Interface
DS-2194	Keyboard Interface
PL-2215	LED Indicator
L-2215	LED Indicator
S-2215	LED Indicator
PL-2213	Format Store
L-2213	Format Store
S-2213	Format Store

Chassis

PL-2115	Heat Sink Filter Assembly (Group 4)
L-2115	Heat Sink Filter Assembly (Group 4)
S-2115	Heat Sink Filter Assembly
PL-3204	Replaceable Parts List - Control Panel Wiring
S-3204	Control Panel Wiring
PL-3205	Replaceable Parts List - Chassis Wiring
S-3205	Chassis Wiring
PL-3070	Replaceable Parts List - Rear Connector Panel Wiring
S-3070	Rear Connector Panel Wiring

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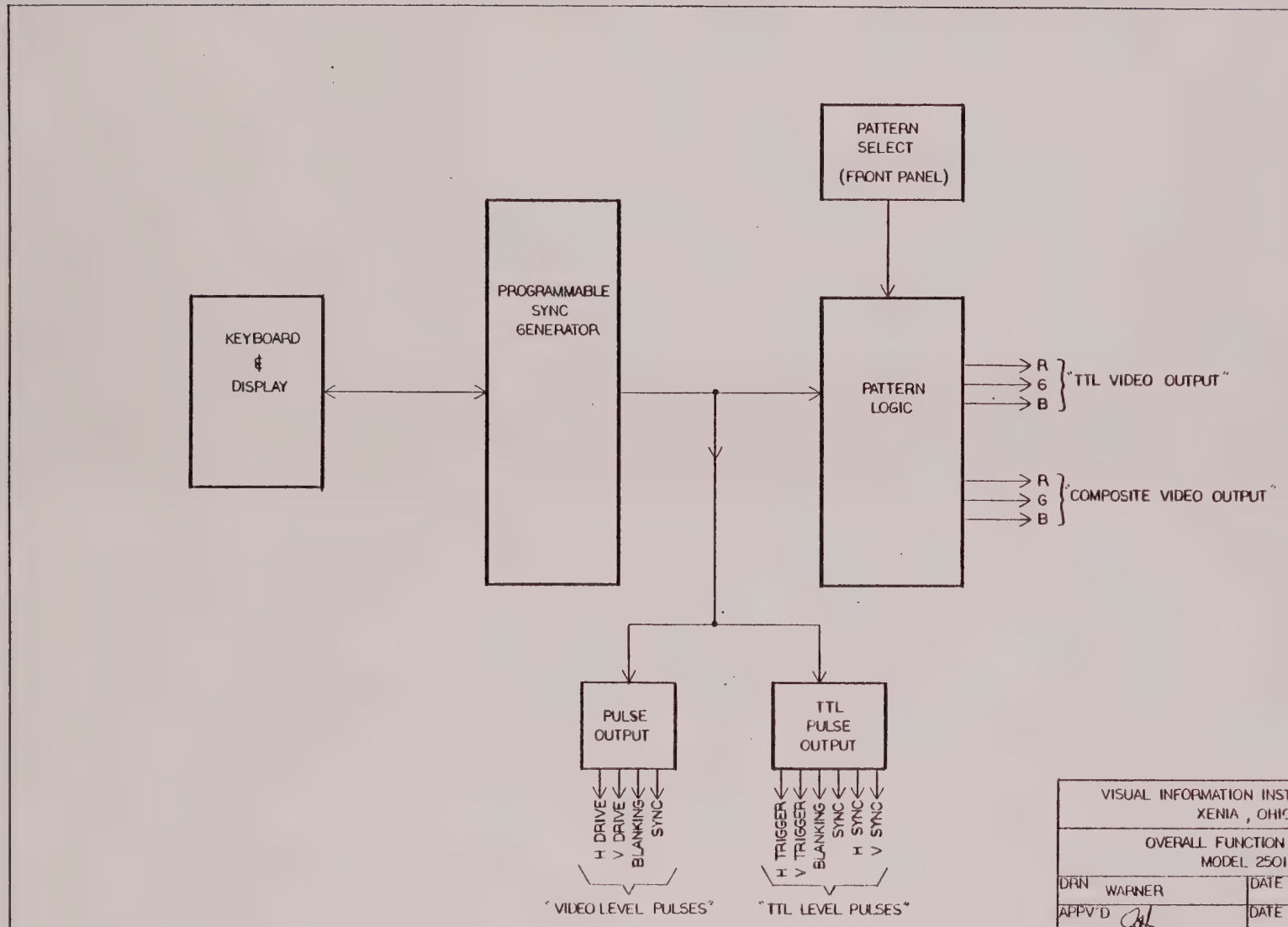
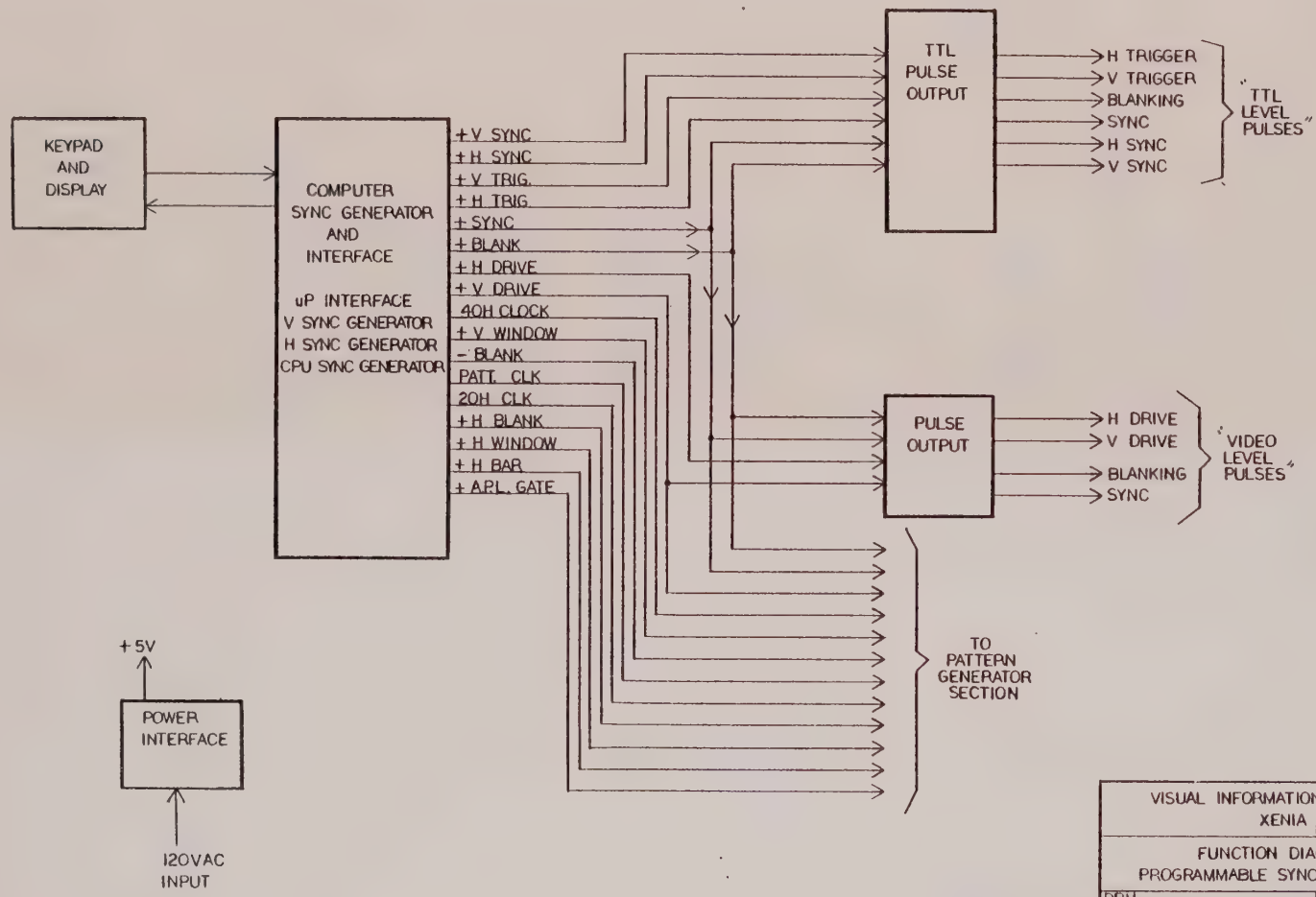


VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
OVERALL FUNCTION DIAGRAM MODEL 2501-H	
DRN WARNER	DATE 3-13-85
APPV'D	DATE 3-15-85
	DWG NO. S-3211
REV.	



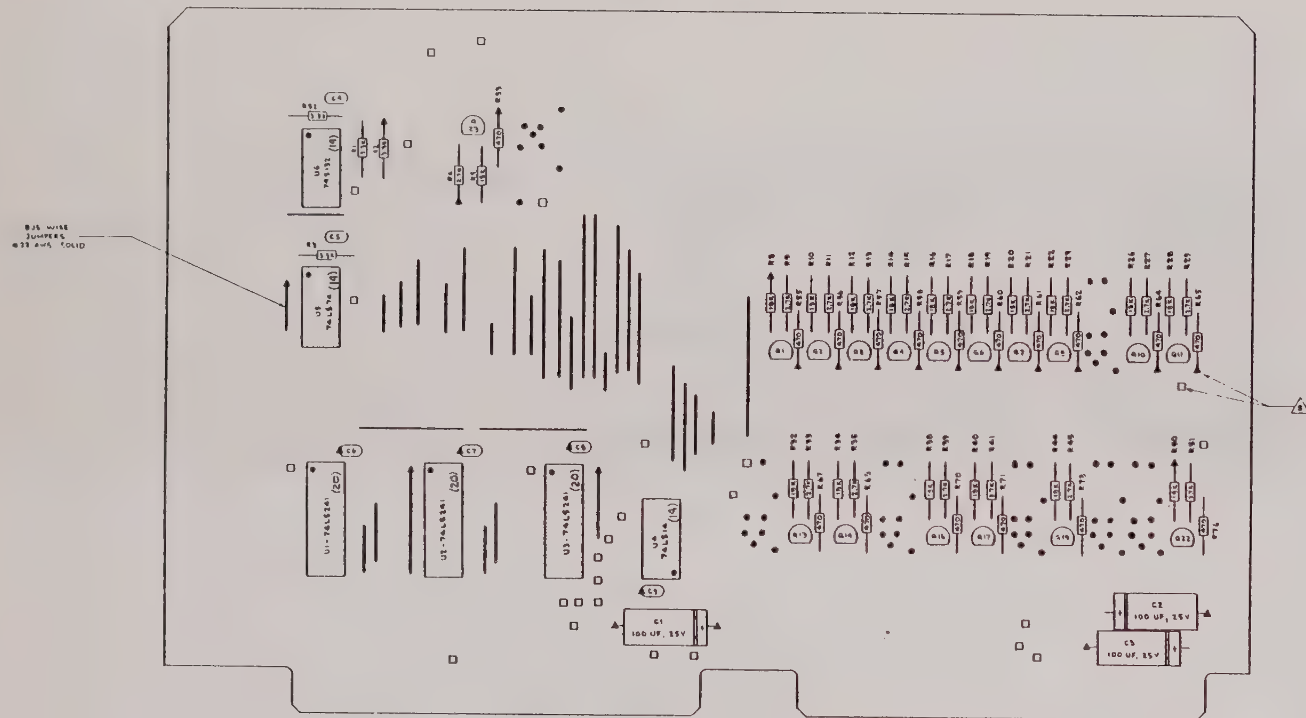
VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
FUNCTION DIAGRAM – MODEL 250I-H PROGRAMMABLE SYNC GENERATOR SECTION	
DRN. D.W.	DATE 11-21-84
APPV'D JH	DATE 3-13-85
REV.	DWG. NO. S-3202

u PROCESSOR INTERFACE
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-2196

ARTWORK REV. A (3/84) 3/14/85 SHT 1 of 1

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	MFR.	Vii DWG.NO.
PCB ASSEMBLY		X	Vii	DL-2196
PCB ARTWORK	COND. SIDE	X	Vii	DB-2196
PCB ARTWORK	COMP. SIDE	X	Vii	DF-2196
PCB SCHEMATIC		X	Vii	DS-2196
DRILL DRAWING		X	Vii	DD-2196
Hole Count		462		
Transistors	2N2369	17	BAS	A-1844
Resistors, Fixed	470 ohms	17	BAS	A-1450
"	2.7K ohms	17	BAS	A-1450
"	3.3K ohms	4	BAS	A-1450
"	18K ohms	17	BAS	A-1450
Capacitors	0.1uf, 50v	6	BAS	A-1455
"	100uf, 25v	3	BAS	A-1458
I.C. Sockets	14 pin	3	BAS	A-1465
"	20 pin	3	BAS	A-1465
I.C.'s	74LS14	1	BAS	
"	74LS74	1	BAS	
"	74LS132	1	BAS	
"	74LS241	3	BAS	
Bus Wire, Jumpers	#22 Awg Solid	32	BAS	
Comp Feed Thru = ▲		27		
Wire Feed Thru = ■	#22 Awg Solid	27		



P2

PIN	FUNCTION (CONDUCTOR SIDE)	PIN	FUNCTION (COMPONENT SIDE)
A	2H CLOCK	1	INT M O ON
B	BLANK	2	EXT M O IN
C	V SYNC	3	CHAR CONT
D	SYNC	4	PATT CLK
E	2H EQUAL	5	H GATE
F	H BLANK	6	H WINDOW
H	2H SEPR	7	
J	H SYNC	8	
K	/ TRIG	9	H DRIVE
L		10	
M	H TRIG	11	BOUNCE IN
N	V DRIVE	12	
P	V GATE	13	
R	H CROSSHAIR	14	
S	V WINDOW	15	
T	V BLANK	16	
U	APL	17	
V	H BAR	18	
W	V B CLK	19	
X		20	CHAR CLK
Y	GND	21	GND
Z	+5V	22	-9V

P1

PIN	FUNCTION (CONDUCTOR SIDE)	PIN	FUNCTION (COMPONENT SIDE)
A		1	+H DRIVE
B	+H TRIG	2	+H SYNC
C	40M CLK	3	+ SYNC
D		4	+H BLANK
E	+V WINDOW	5	+H WINDOW
F	- BLANK	6	+ BLANK
H		7	+V DRIVE
J	+V SYNC	8	+V TRIG
K		9	
L		10	+H BAR
M	EXT M O IN	11	+ APL GATE
N	INT M O ON	12	CHAR CONT.IN
P	PATT CLK	13	CHAR CLK OUT
R	20M CLK	14	
S		15	
T		16	
U		17	
V		18	
W		19	
X		20	
Y	GND	21	GND
Z	+5V	22	-5V

REF DESIG	LAST	NOT
U	U6	
R	R76	
C	C9	
Q	Q24	

NOTES:

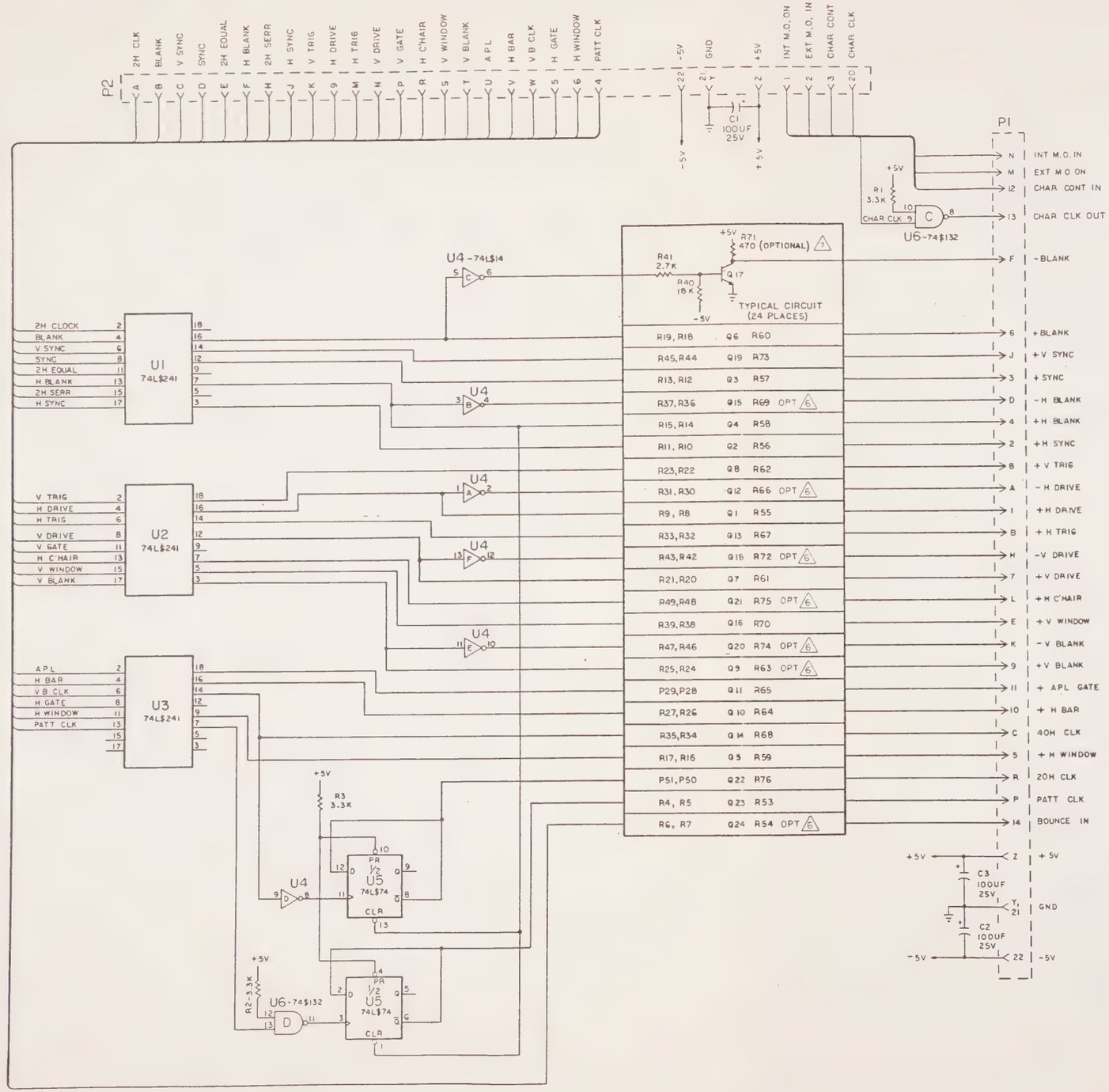
1) FOR PARTS LIST SEE P/L-2196
2) FOR SCHEMATIC SEE DS-2196
3) ALL RESISTORS = 1/4W, ±10% TOL
4) C4 THRU C8 = 0.1 UF, 50V
5) SOLDERING IS REQUIRED ON BOTH SIDES OF P.C BD
▲ = COMP LEAD FEED THRU
□ = #22 AWG WIRE FEED THRU
6. ALL TRANSISTORS = 2N5134.

GROUP 1

VISUAL INFORMATION INSTITUTE, INC.
XENIA, OHIO

U PROCESSOR INTERFACE COMPONENT LAYOUT

DWN PAT AUTONICK — DATE 8-29-84
APPVD — DATE 9-4-84
REV. 3-14-85
PC ART REV A (3-84)
DWG NO DL-2196



R19, R18	Q6	R60	
R45, R44	Q19	R73	
R13, R12	Q3	R57	
R37, R36	Q15	R69	OPT 6
R15, R14	Q4	R58	
R11, R10	Q2	R56	
R23, R22	Q8	R62	
R31, R30	Q12	R66	OPT 6
R9, R8	Q1	R55	
R33, R32	Q13	R67	
R43, R42	Q16	R72	OPT 6
R21, R20	Q7	R61	
R49, R48	Q21	R75	OPT 6
R39, R38	Q16	R70	
R47, R46	Q20	R74	OPT 6
R25, R24	Q9	R63	OPT 6
P29, P28	Q11	R65	
R27, R26	Q10	R64	
R35, R34	Q14	R68	
R17, R16	Q5	R59	
P51, P50	Q22	R76	
R4, R5	Q23	R53	
R6, R7	Q24	R54	OPT 6

POWER SUPPLY CHART

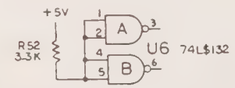
	+5	GND
74L$241	20	10
74$132	14	7
74L$14	14	7
74L$74	14	7

REFERENCE DESIGNATOR CHART

REF. DESIG	LAST	NOT
U	U6	
R	R76	
C	C9	
Q	Q24	
P	P2	

NOTES (UNLESS OTHERWISE SPECIFIED)

1) ALL RESISTORS ARE: 1/4W, ±10% TOL.
2) C4 THRU C8: 0.1 UF, 50V. (NOT SHOWN)
3) TRANSISTORS: 2N5134.
4) COMP LAYOUT-DL-2196.
5) UNUSED GATES:



6 FOR OPT PARTS PER GROUP LISTING - REFER TO INDIVIDUAL GROUP ASS'Y DWGS L-2196 (GROUP 1).

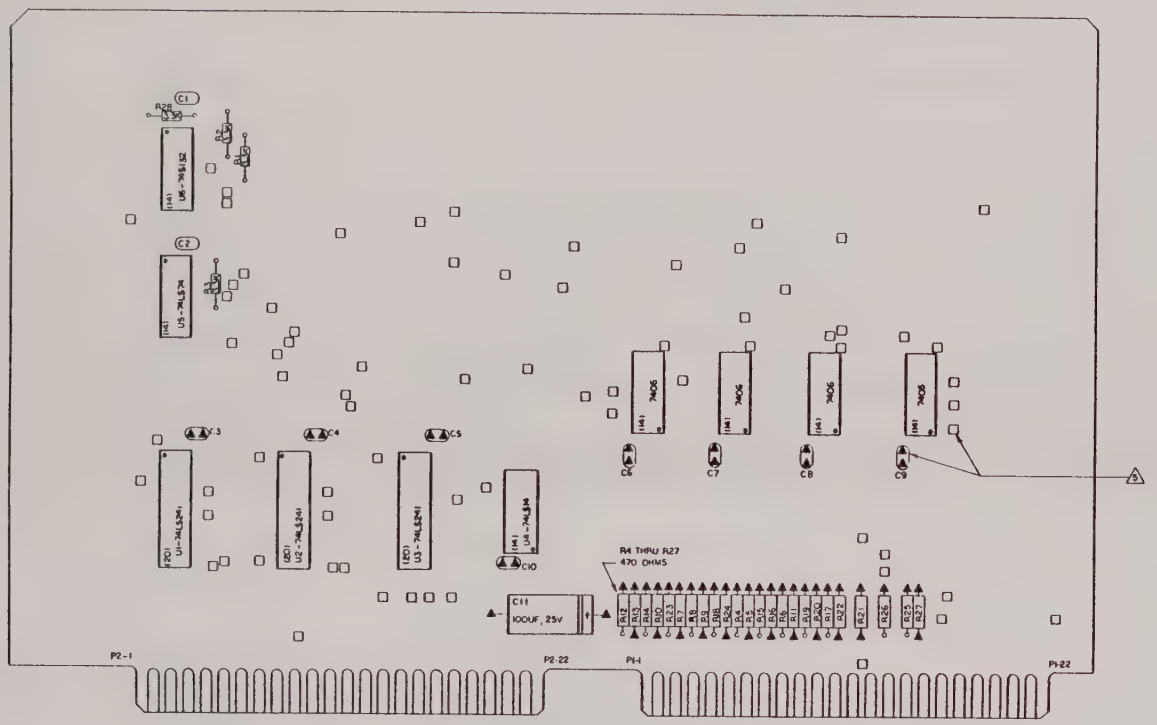
7 PULL UP RESISTORS ON ALL OUTPUTS ARE OPTIONAL.

VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO USA	
4 PROCESSOR INTERFACE SCHEMATIC	
DRN PAT ANTONICK	DATE 8-29-84
APPV'D	DATE 9-30-84
PC REV A (3-84)	DWG NO DS-2196
REV. 3-14-85	

uP INTERFACE
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST — PL-4015
ARTWORK REV. A (10/84) — 1/16/85 — SHT 1 of 1

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/ TYPE	QTY	MFR	Vii DWG.NO.
REF.	SCHEMATIC			Vii	DS-4015
REF.	COMP. LAYOUT (ASS'Y)			Vii	DL-4015
REF.	PC ARTWORK (COND. SIDE)			Vii	DB-4015
REF.	PC ARTWORK (COMP. SIDE)			Vii	DF-4015
REF.	DRILL DWG.			Vii	DD-4015
R4 - R27	Resistor, Fixed	470 ohms	24	BAS	A-1450
R1,2,3,28	Resistor, Fixed	3.3K ohms	4	BAS	A-1450
C1 - C10	Capacitor	0.1uf, 50v	10	BAS	A-1455
C11	Capacitor	100uf, 25v	1	BAS	A-1458
- -	I.C. Socket	14 pin	7	BAS	A-1465
- -	I.C. Socket	20 pin	3	BAS	A-1465
U7 - U10	I.C.	7406	4	BAS	
U4	I.C.	74LS14	1	BAS	
U5	I.C.	74LS74	1	BAS	
U6	I.C.	74S132	1	BAS	
U1,2,3	I.C.	74LS241	3	BAS	
- -	Comp. Feed Thru's		54	BAS	
- -	Wire Feed Thru's	#22 Awg Solid	73	BAS	



REFERENCE DESIGNATOR CHART		
REF DESG	LAST	NOT
U	U10	
R	R28	
C	C11	

NOTES:

1) FOR PARTS LIST SEE P/L-4015
2) FOR SCHEMATIC SEE DS-4015
3) ALL RESISTORS = 1/4W ; ±10% TOL
4) C1 THRU C10 = 0.1UF, 50V
5) SOLDERING IS REQUIRED ON BOTH SIDES OF P.C. BD.
▲ = COMP. LEAD FEED THRU
□ = #22 AWG WIRE FEED THRU.

P2

CONDUCTOR SIDE			COMPONENT SIDE
PIN	FUNCTION	PIN	FUNCTION
A	2H CLOCK	1	INT. M.O. ON
B	BLANK	2	EXT. M.O. ON
C	V. SYNC	3	CHAR. CONT.
D	SYNC	4	PART. CLK
E	2H EQUAL	5	H. GATE
F	H. BLANK	6	H. WINDOW
H	2H SERR.	7	---
J	H. SYNC	8	---
K	V. TRIG.	9	H. DRIVE
L	---	10	---
M	H. TRIG.	11	BOUNCE IN
N	V. DRIVE	12	---
P	V. GATE	13	---
R	H. CROSSHAIR	14	---
S	V. WINDOW	15	---
T	V. BLANK	16	---
U	A.P.L	17	---
V	H. BAR	18	---
W	V. B. CLK	19	---
X	---	20	CHAR. CLK
Y	GND	21	GND
Z	+5V	22	+5V

P1

CONDUCTOR SIDE			COMPONENT SIDE
PIN	FUNCTION	PIN	FUNCTION
A	+H DRIVE	1	+H DRIVE
B	+H TRIG	2	+H SYNC
C	40H CLK	3	+SYNC
D	-H BLANK	4	+H BLANK
E	+V WINDOW	5	+V WINDOW
F	-BLANK	6	+BLANK
H	-V DRIVE	7	+V DRIVE
J	+V SYNC	8	+V TRIG
K	-V BLANK	9	+V BLANK
L	+H CROSSHAIR	10	+H BAR
M	EXT. M.O. IN	11	+A.P.L. GATE
N	INT. M.O. ON	12	CHAR. CONT. IN
P	PART. CLK	13	CHAR. CONT. OUT
R	20H CLK	14	BOUNCE OUT
S	---	15	---
T	---	16	---
U	---	17	---
V	---	18	---
W	---	19	---
X	---	20	---
Y	GND	21	GND
Z	+5V	22	+5V

VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
U PROCESSOR INTERFACE COMPONENT SIDE	
DRN WARNER	DATE 1-16-85
APP'D [illegible]	DATE 1-22-85
PC ART REV A(10-84)	DWG NO
REV	DI-4015

POSITION 16B uP INTERFACE (Group 0)

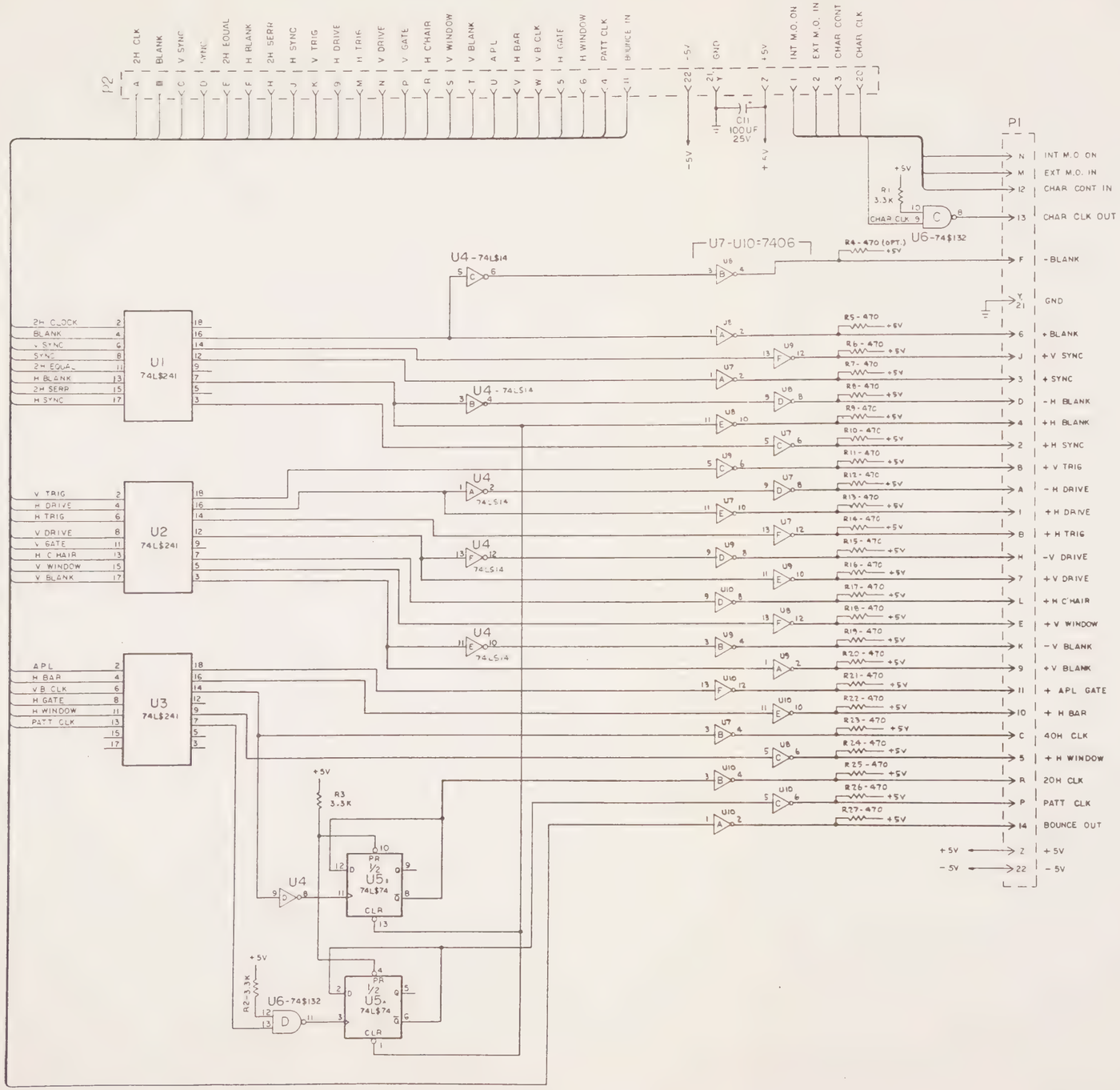
MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
A	--	
B	+H TRIG	(TTL PULSE OUTPUT, PIN B)
C	40H CLOCK	(VIDEO CLOCK, PIN D)
D	--	
E	+V WINDOW	(PATTERN LOGIC, PIN D)
F	-BLANK	(PATTERN LOGIC, PIN E)(VIDEO CLOCK, PIN B)
H	--	
J	+V SYNC	(TTL PULSE OUTPUT, PIN J)
K	--	
L	--	
M	--	
N	+5v.	(uP INTERFACE (P1), PIN Z)
P	V BAR CLOCK . . .	(CLOCKED BAR/DOT, PINS E, S)
R	20H CLOCK	(GRAY SCALE SELECT, PIN E)(CLOCKED COLOR BAR, PIN H)
S	--	
T	--	
U	--	
V	--	
W	--	
X	--	
Y	GROUND	(uP INTERFACE (P1), PIN 21)(CLOCKED BAR/DOT, GROUND)
Z	+5v.	(uP INTERFACE (P1), PIN N)

POSITION 16B uP INTERFACE (Group 0)

MODEL 2501-H
WIRING INTERCONNECTIONS (cont.)

CONNECTOR PIN	FUNCTION	DESTINATION
1	+H DRIVE	(PULSE OUTPUT, PIN B)
2	+H SYNC	(TTL PULSE OUTPUT, PIN H)
3	+SYNC	(TTL PULSE OUTPUT, PIN E)
4	+H BLANK	(CLOCKED BAR/DOT, PIN D)(VIDEO CLOCK, PIN F)(GRAY SCALE SELECT, PIN D) (CLOCKED COLOR BAR, PIN J)(CHARACTER, PIN X)
5	+H WINDOW	(PATTERN LOGIC, PIN X)
6	+BLANK	(TTL PULSE OUTPUT, PIN D)(PULSE OUTPUT, PIN D)(RESOLUTION (7C,9C), PIN R) (CHARACTER, PIN Z)(CLOCKED BAR/DOT, PIN J)(RESOLUTION CONTROL, PIN C)
7	+V DRIVE	(PULSE OUTPUT, PIN C)(CHARACTER, PIN U)
8	+V TRIG	(TTL PULSE OUTPUT, PIN C)
9	--	
10	+H BAR	(CLOCKED BAR/DOT, PIN C)
11	+APL GATE	(PATTERN LOGIC, PIN C)
12	--	
13	--	
14	--	
15	--	
16	--	
17	--	
18	--	
19	--	
20	--	
21	GROUND	(uP INTERFACE (P1), PIN Y)(CLOCKED BAR/DOT, GROUND)
22	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)



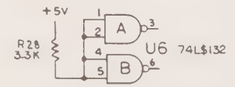
POWER SUPPLY CHART

	+5	GND
74LS241	20	10
74S132	14	7
74LS14	14	7
74LS74	14	7
74LS06	14	7

REFERENCE DESIGNATOR CHART

REF DESIG	LAST	NOT
U	U10	
R	R28	
C	C11	
P	P2	

NOTES (UNLESS OTHERWISE SPECIFIED)
1) ALL RESISTORS ARE: 1/4W, ±10% TOL.
2) C2 THRU C11: 0.1 UF, 50V. (NOT SHOWN)
3) TRANSISTORS:
4) COMP LAYOUT-DL-4015.
5 UNUSED GATES:



VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO USA	
μ PROCESSOR INTERFACE SCHEMATIC	
DRN PAT ANTONICK	DATE 11-19-84
APPV'D	DATE 11-27-84
PC REV A (10-84)	DWG NO DS-4015
REV. 1-16-85	

VERTICAL SYNC GENERATOR
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST
ARTWORK REV. A (3/84)

11/8/84

PL-2192
SHT 1 OF 2

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/ TYPE	QTY	MFR	Vii DWG. NO.
REF.	SCHEMATIC			Vii	DS-2192
REF.	COMPONENT LAYOUT (ASS'Y)			Vii	DL-2192
REF.	PC ARTWORK (COND. SIDE)			Vii	DB-2192
REF.	PC ARTWORK (COMP. SIDE)			Vii	DF-2192
REF.	DRILL DWG.			Vii	DD-2192
Q1	Transistor	2N2369	1	BAS	
R1	NOT USED		-		
R5	Resistor, Fixed	2.7K ohms	1	BAS	A-1450
R2, 3	Resistor, Fixed	3.3K ohms	2	BAS	A-1450
R4	Resistor, Fixed	18K ohms	1	BAS	A-1450
RN1	Resistor Network-SIP	1K (6 pin)	1	BAS	A-1873
RN2	Resistor Network-SIP	1K (10 pin)	1	BAS	A-1873
RN3	Resistor Network-SIP	3.3K (8 pin)	1	BAS	A-1873
RN4, 5	NOT USED		-		
RN6	Resistor Network-SIP	3.3K (10 pin)	1	BAS	A-1873
C1	Capacitor	100uf, 25v	1	BAS	
C2 thru C28	Capacitor	0.1uf, 50v	26	BAS	A-1455
C3	NOT USED		-		
- -	I.C. Socket	14 pin	5	BAS	A-1465
- -	I.C. Socket	16 pin	7	BAS	A-1465
- -	I.C. Socket	20 pin	10	BAS	A-1465
- -	I.C. Socket	24 pin	2	BAS	A-1465
- -	I.C. Socket	48 pin	1	BAS	A-1465
U27	I.C.	74LS00	1	BAS	
U19	I.C.	74LS04	1	BAS	
U18	I.C.	74LS32	1	BAS	
U21	I.C.	74LS74	1	BAS	
U3,4,5	I.C.	74LS163	3	BAS	
U14	I.C.	74LS541	1	BAS	
U13	I.C.	74LS164	1	BAS	
U9,10,15,16	I.C.	74LS367	4	BAS	
U11,12	I.C.	74LS374	2	BAS	
U17	I.C.	74LS640	1	BAS	
U20	I.C.	74LS682	1	BAS	
U1,2	I.C.	PAL16L8	2	BAS	
U25,26	I.C.	52B13	2	BAS	
U24	I.C.	68230	1	BAS	
U6,7,8	I.C.	IMS1420P-10L	3	BAS	
U22, U23	NOT USED		-		

VERTICAL SYNC GENERATOR
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-2192

ARTWORK REV. A (3/84) 11/8/84 SHT 2 OF 2

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/ TYPE	QTY	MFR	Vii DWG. NO.
J1	NOT USED		-		
J2	Connector (Header)	12 pin (6 dbl row)	1	BAS	

REVISIONS					
SYM	DATE	DESCRIPTION	DW	CHK	DATE
	11-8-84	CORRECTED VENEC54	DW		

POWER SUPPLY CHART

	+5V	GND
PAL16L8	20	10
74LS163	16	8
IMS1420L	20	10
74LS367	16	8
74LS374	20	10
74LS164	14	7
74LS541	20	10
74LS640	20	10
74LS32	14	7
74LS04	14	7
74LS682	20	10
74LS74	14	7
74LS00	14	7
74LS244	20	10
74LS14	14	7
68230	12	38
52813	24	12

REFERENCE DESIGNATOR CHART

REF DESIG	LAST	NOT
U	U27	
C	C28	
Q	Q1	
R	R5	
RN	RN6	
J	J2	
P	P2	

NOTES: UNLESS OTHERWISE SPECIFIED

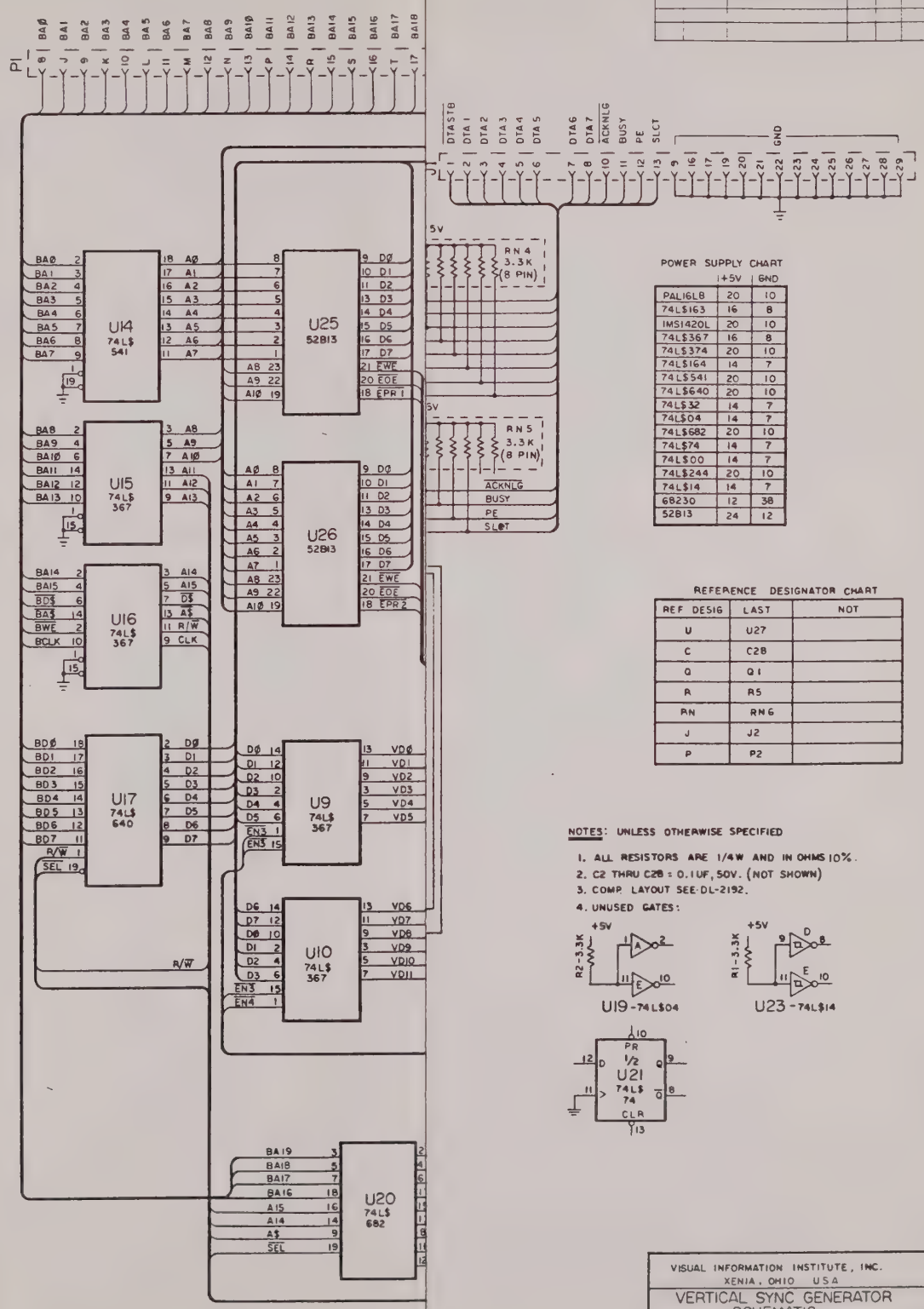
1. ALL RESISTORS ARE 1/4W AND IN OHMS 10%
2. C2 THRU C28 = 0.1UF, 50V. (NOT SHOWN)
3. COMP. LAYOUT SEE DL-2192.
4. UNUSED GATES:

U19-74LS04 U23-74LS14

U21 74LS74 PR 1/2 CLR

VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO USA		
VERTICAL SYNC GENERATOR SCHEMATIC		
DRN PAT ANTONICK	DATE 3-22-84	
APPV'D	DATE 9-20-84	
P.C. ART REV.	DWG NO. DS-2192	

REVISIONS					
SYM	DATE	DESCRIPTION	DW	CH'K	DATE
	11-6-84	CORRECTED VEN & $\overline{CS4}$	DW		



POWER SUPPLY CHART

	+5V	GND
PAL16L8	20	10
74L$163	16	8
IMS1420L	20	10
74L$367	16	8
74L$374	20	10
74L$164	14	7
74L$541	20	10
74L$640	20	10
74L$32	14	7
74L$04	14	7
74L$682	20	10
74L$74	14	7
74L$00	14	7
74L$244	20	10
74L$14	14	7
68230	12	38
52B13	24	12

REFERENCE DESIGNATOR CHART

REF DESIG	LAST	NOT
U	U27	
C	C28	
Q	Q1	
R	R5	
RN	RN6	
J	J2	
P	P2	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS 10%.
2. C2 THRU C28 = 0.1UF, 50V. (NOT SHOWN)
3. COMP. LAYOUT SEE DL-2192.
4. UNUSED GATES:

VISUAL INFORMATION INSTITUTE, INC.
XENIA, OHIO USA

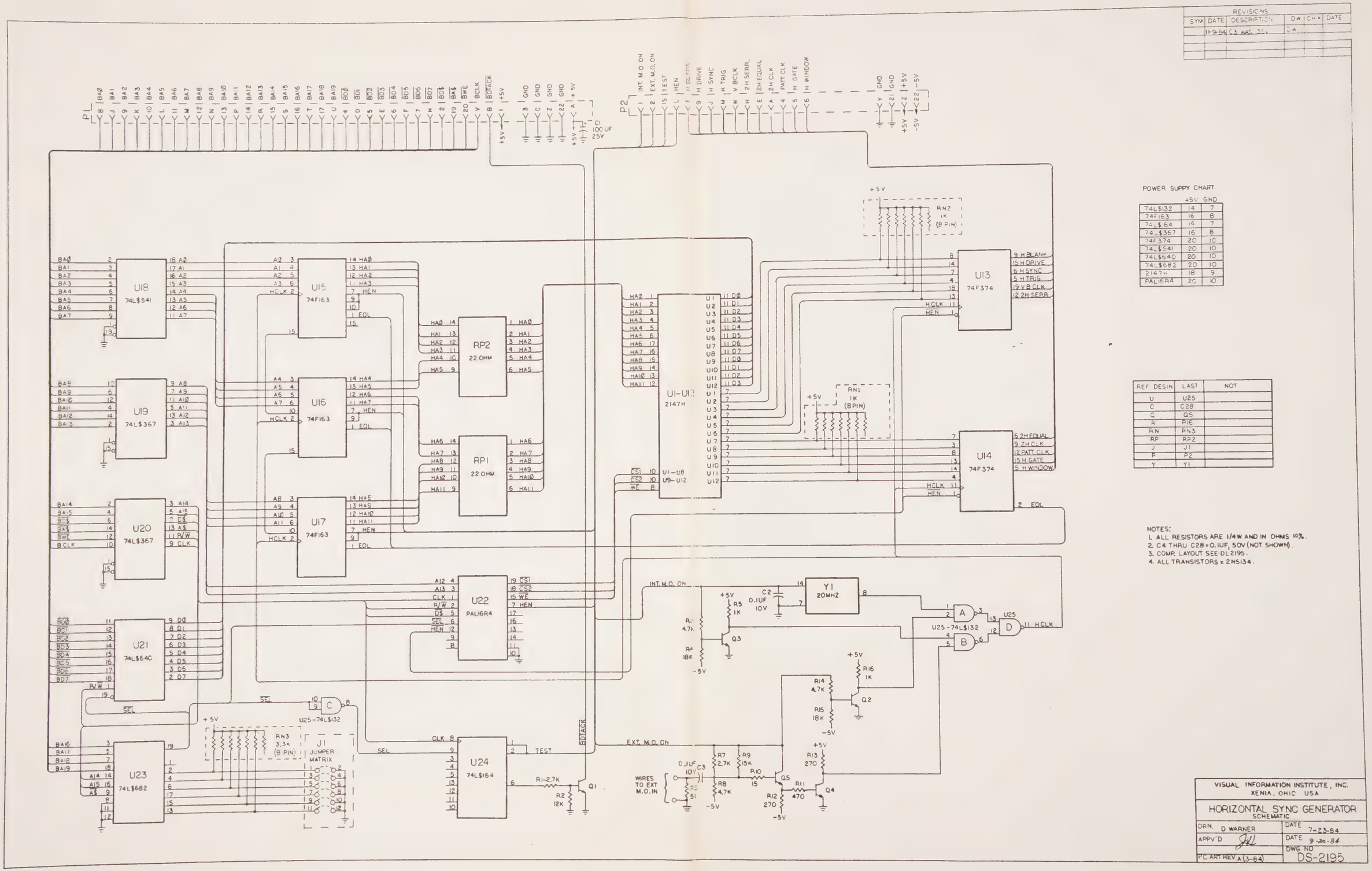
VERTICAL SYNC GENERATOR SCHEMATIC

DRN PAT ANTONICK	DATE 5-22-84
APPV'D [signature]	DATE 9-20-84
P.C. ART REV	DWG NO DS-2192

HORIZONTAL SYNC GENERATOR
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST
REV. ARTWORK A (3/84) 11/9/84

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/ TYPE	QTY	MFR	Vii DWG. NO.
REF.	SCHEMATIC			Vii	DS-2195
REF.	COMPONENT LAYOUT (ASS'Y)			Vii	DL-2195
REF.	PC ARTWORK (COND. SIDE)			Vii	DB-2195
REF.	PC ARTWORK (COMP. SIDE)			Vii	DF-2195
REF.	DRILL DWG.			Vii	DD-2195
Q1 thru Q5	Transistor	2N5134	5	BAS	A-1797
R10	Resistor, Fixed	15 ohms	1	BAS	A-1450
R6	Resistor, Fixed	51 ohms	1	BAS	A-1450
R12, 13	Resistor, Fixed	270 ohms	2	BAS	A-1450
R11	Resistor, Fixed	470 ohms	1	BAS	A-1450
R5, 16	Resistor, Fixed	1K ohms	2	BAS	A-1450
R1, 7	Resistor, Fixed	2.7K ohms	2	BAS	A-1450
R3, 8, 14	Resistor, Fixed	4.7K ohms	3	BAS	A-1450
R2	Resistor, Fixed	12K ohms	1	BAS	A-1450
R9	Resistor, Fixed	15K ohms	1	BAS	A-1450
R4, 15	Resistor, Fixed	18K ohms	2	BAS	A-1450
RN1, 2	Resistor Network-SIP	1K (8 pin)	2	BAS	A-1873
RN3	Resistor Network-SIP	3.3K (8 pin)	1	BAS	A-1873
RP1, 2	Resistor Pack	22 ohms	2	BAS	
C1	Capacitor	100uf, 25v	1	BAS	A-1458
C2, C3	Capacitor	0.1uf, 10v	2	BAS	A-1455
C4 thru C28	Capacitor	0.1uf, 50v	25	BAS	A-1455
- -	I.C. Socket	14 pin	2	BAS	A-1465
- -	I.C. Socket	16 pin	5	BAS	A-1465
- -	I.C. Socket	18 pin	12	BAS	A-1465
- -	I.C. Socket	20 pin	6	BAS	A-1465



POWER SUPPY CHART

	+5V	GND
74LS132	14	7
74F163	16	8
74LS64	14	7
74LS367	16	8
74F374	20	10
74LS541	20	10
74LS640	20	10
74LS682	20	10
2147H	18	9
PAL16R4	20	10

REF DESIN	LAST	NOT
U	U25	
C	C28	
Q	Q5	
R	R16	
RN	RN3	
RP	RP2	
J	J1	
P	P2	
Y	Y1	

NOTES:
1. ALL RESISTORS ARE 1/4W AND IN OHMS 10%.
2. C4 THRU C28 = 0.1UF, 50V (NOT SHOWN).
3. COMP. LAYOUT SEE DL2195.
4. ALL TRANSISTORS = 2N5134.

REVISIONS

SYM	DATE	DESCRIPTION	DW	CHK	DATE
	11-9-84	C3 WAS 35V	DW		

VISUAL INFORMATION INSTITUTE, INC.
XENIA, OHIO USA

HORIZONTAL SYNC GENERATOR
SCHEMATIC

DRN. D WARNER	DATE 7-23-84
APPV'D [signature]	DATE 9-20-84
PC ART REV A (3-84)	DWG NO DS-2195

H/V MPU CONTROLLED SYNC GENERATOR
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-2221

ARTWORK REV. A (1/85) 3/25/85 SHT 1 of 2

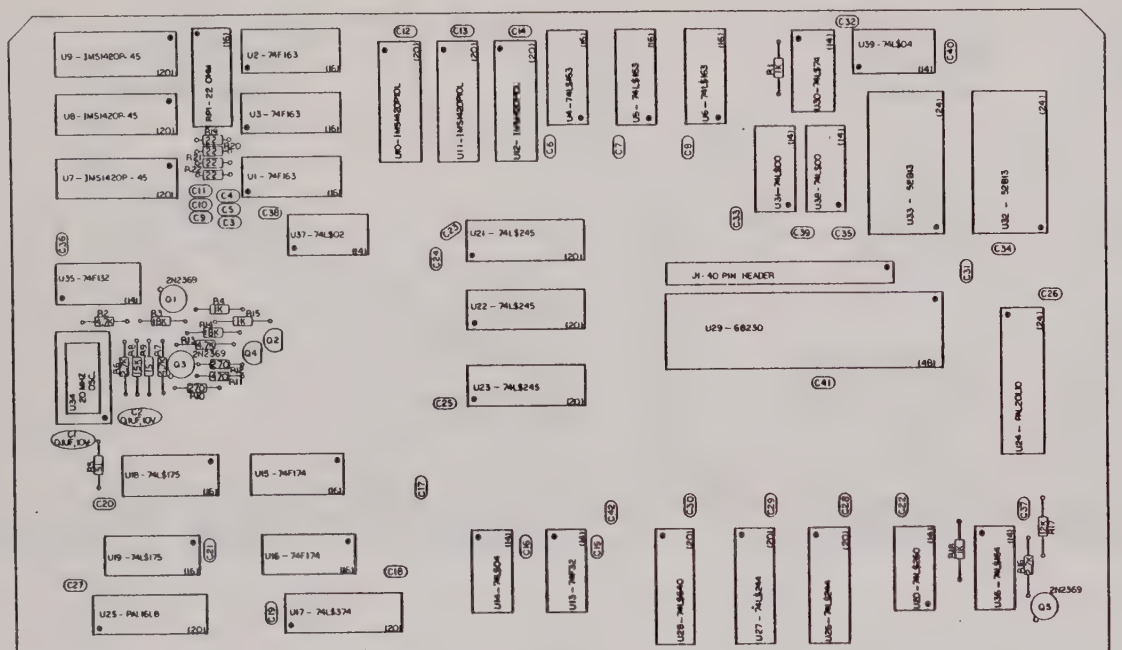
DESCRIPTION	VALUE/TYPE	QTY/GROUP 0	MFR.	Vii DWG.NO.
PCB ASSEMBLY		X	Vii	DL-2221
PCB ARTWORK	COND. SIDE	X	Vii	DB-2221
PCB ARTWORK	COMP. SIDE	X	Vii	DF-2221
PCB SCHEMATIC		X	Vii	DS-2221
DRILL DRAWING		X	Vii	DD-2221
Transistors	2N5134	2	BAS	A-1844
"	2N2369	3	BAS	
Resistors, Fixed	15 ohms	1	BAS	A-1450
"	22 ohms	4	BAS	A-1450
"	51 ohms	1	BAS	A-1445
"	270 ohms	2	BAS	A-1450
"	470 ohms	1	BAS	A-1450
"	1K ohms	4	BAS	A-1450
"	2.7K ohms	2	BAS	A-1450
"	4.7K ohms	3	BAS	A-1450
"	12K ohms	1	BAS	A-1450
"	15K ohms	1	BAS	A-1450
"	18K ohms	2	BAS	A-1450
Resistor Pack	22 ohms (16 pin)	1	BAS	
Capacitors	0.1uf, 10v.	2	BAS	A-1455
"	0.1uf, 50v	34	BAS	A-1455
I.C. Sockets	14 pin	10	BAS	A-1465
"	16 pin	10	BAS	A-1465
"	20 pin	14	BAS	A-1465
"	24 pin	3	BAS	A-1465
"	48 pin	1	BAS	A-1465

H/V MPU CONTROLLED SYNC GENERATOR
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-2221

ARTWORK REV. A (1/85) 3/25/85 SHT 2 of 2

DESCRIPTION	VALUE/TYPE	QTY/GROUP 0	MFR.	Vii DWG.NO.
I.C.'s	74F32	1	BAS	
"	74F132	1	BAS	
"	74F163	3	BAS	
"	74F174	2	BAS	
"	74LS00	2	BAS	
"	74LS02	1	BAS	
"	74LS04	2	BAS	
"	74LS74	1	BAS	
"	74LS163	3	BAS	
"	74LS164	1	BAS	
"	74LS175	2	BAS	
"	74LS244	2	BAS	
"	74LS245	3	BAS	
"	74LS260	2	BAS	
"	74LS374	1	BAS	
"	74LS640	1	BAS	
"	IMS1420P10	3	BAS	
"	IMS1420P45	3	BAS	
"	PAL16L8	1	BAS	
"	PAL20L10	1	BAS	
"	52B13	2	BAS	
"	68230	1	BAS	
"	20 mHz Osc.	1	BAS	



P2

PIN	COMPONENT SIDE FUNCTION	CONDUCTOR SIDE PIN	CONDUCTOR SIDE FUNCTION
1	INT. MOJIN	A	24 CLK
2	EXT. MOJIN	B	BLANK
3	- - -	C	V SYNC
4	MULTI CLK	D	SYNC
5	H GATE	E	2H CLK
6	H WINDOW	F	H BLANK
7	- - -	H	2H SERR
8	- - -	J	H SYNC
9	H DRIVE	K	V TRIG
10	- - -	L	HEN
11	BOUNCE IN	M	H TRIG
12	- - -	N	V DRIVE
13	- - -	P	V GATE
14	- - -	R	H CROSSHAIR
15	- - -	S	V WINDOW
16	- - -	T	V BLANK
17	- - -	U	A.S.L.
18	- - -	V	H BAR
19	- - -	W	V BAR
20	- - -	X	- - -
21	GND	Y	GND
22	-5V	Z	+5V

P1

PIN	COMPONENT SIDE FUNCTION	CONDUCTOR SIDE PIN	CONDUCTOR SIDE FUNCTION
1	+5V	A	+5V
2	BD3	B	BD7
3	GND	C	GND
4	BD3	D	BD7
5	BD2	E	BD3
6	BD2	F	BD5
7	BD6	H	BD7
8	BA9	J	BA1
9	BA2	K	BA3
10	BA4	L	BA7
11	BA5	M	BA7
12	BA8	N	BA9
13	BA16	P	BA11
14	BA12	R	BA13
15	BA14	S	BA15
16	BA16	T	BA17
17	BA18	U	BA19
18	- - -	V	R CLK
19	BA1	W	RESET
20	BA6	X	- - -
21	- - -	Y	- - -
22	GND	Z	GND

REFERENCE DESIGNATOR CHART

REF. DESIG	LAST	NOT
C	C42	
U	U39	
R	R22	
RP	RP1	
Q	Q5	
J	J1	
P	P2	

NOTES:
1) FOR PARTS LIST SEE PL-2221
2) FOR SCHEMATIC SEE DS-2221
3) ALL RESISTORS = 1/4W ; ±10% TOL.
4) ALL TRANSISTOR = 2N5134 UNLESS NOTED
5) C3 THRU C42 = 0.1UF, 50V

VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
H/V MPU CONTROLLED SYNC GEN. COMPONENT LAYOUT	
DRN WARNER	DATE 3-23-85
APP'D	DATE 3-27-85
PC APD REV A (1-85)	DWG NO.
REV	D1-2221

POWER SUPPLY CHART

	+5V	GND
74LS138	16	8
74LS169	16	8
74F 32	14	7
52B13	24	12
74LS00	14	7
74LS74	14	7
6B23C	12	36
74LS640	20	10
74LS244	20	10
PAL16L8	20	10
PAL20L10	24	12
74LS245	20	10
74.3250	14	7
74LS175	16	8
74LS374	20	10
74F174	16	8
74LS04	14	7
74F38	14	7
IMS1420P10L	20	10
IMS1420R45	20	10
74LS163	16	8
74F163	16	8

REFERENCE DESIGNATOR CHART

REF DESIG	LAST	NOT
U	U39	
C	C42	
G	Q5	
R	R22	
RP	RP1	
J	J1	
P	P2	

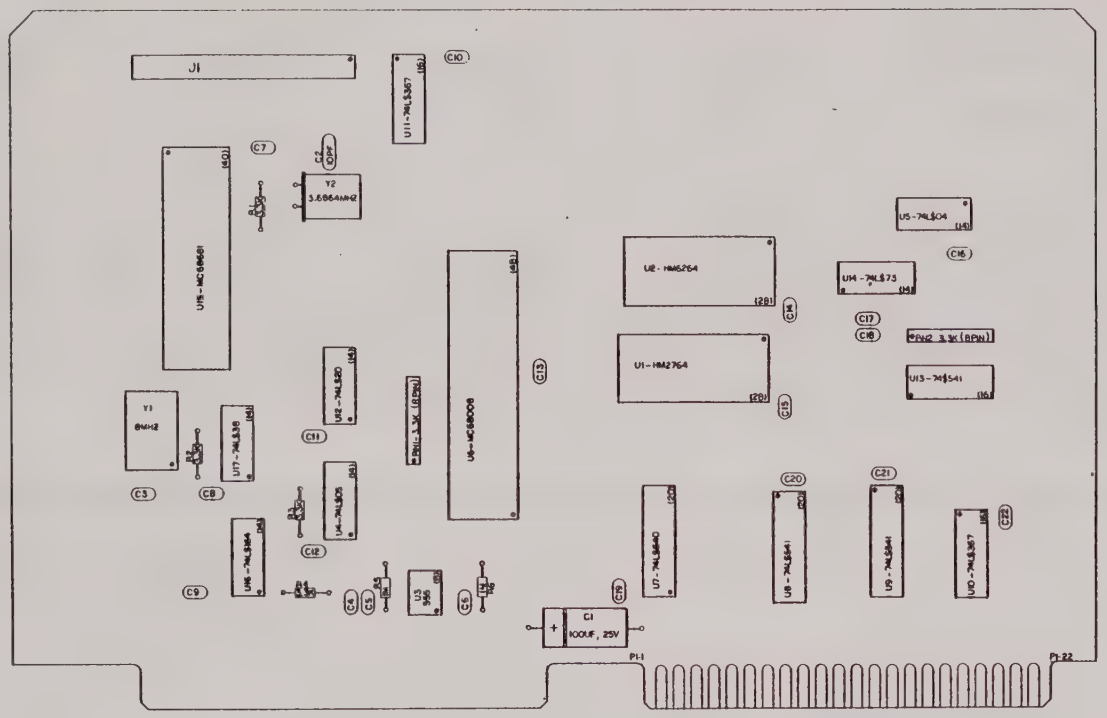
NOTES: UNLESS OTHERWISE SPECIFIED
1) ALL RESISTORS = 1/4W AND IN OHMS 10%
2) ALL TRANSISTORS = 2N5134, UNLESS NOTED
3) C3 THRU C42 = 0.1UF, 50V (NOT SHOWN)
4) COMP LAYOUT SEE DL-2221
5) FOR PARTS LIST SEE PL-2221

VISUAL INFORMATION INSTITUTE, INC XENIA, OHIO	
H/V MPU CONTROLLED SYNC GEN. SCHEMATIC	
DWN WARNER	DATE 3-25-85
APP'D	DATE 3-27-85
PC ART REV A (1-85)	DWG NO DS-2221
REV	

CPU SYNC GENERATOR
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST — PL-2190
ARTWORK REV. A (3/84) — 11/8/84 — SHT 1 OF 1

REFERENCE DESIGNATOR	DESCRIPTION	VALUE\ TYPE	QTY	MFR	Vii DWG. NO.
REF.	SCHEMATIC			Vii	DS-2190
REF.	COMPONENT LAYOUT (ASS'Y)			Vii	DL-2190
REF.	PC ARTWORK (COND. SIDE)			Vii	DB-2190
REF.	PC ARTWORK (COMP. SIDE)			Vii	DF-2190
REF.	DRILL DWG.			Vii	DD-2190
R1,2,3,4	Resistor, Fixed	3.3K ohm	4	BAS	A-1450
R5,6	Resistor, Fixed	1 meg ohm	2	BAS	A-1450
RN1,2	Resistor Network-SIP	3.3K (8 pin)	2	BAS	A-1873
C1	Capacitor	100uf, 25v	1	BAS	A-1458
C2	Capacitor	10 pf	1	BAS	A-1454
C3 thru C22	Capacitor	0.1uf, 50v	20	BAS	A-1455
- -	I.C. Socket	8 pin	1	BAS	A-1465
- -	I.C. Socket	14 pin	6	BAS	A-1465
- -	I.C. Socket	16 pin	3	BAS	A-1465
- -	I.C. Socket	20 pin	3	BAS	A-1465
- -	I.C. Socket	28 pin	2	BAS	A-1465
- -	I.C. Socket	40 pin	1	BAS	A-1465
- -	I.C. Socket	48 pin	1	BAS	A-1465
U1	I.C.	HM2764	1	BAS	
U2	I.C.	HM6264	1	BAS	
U3	I.C.	555	1	BAS	
U4	I.C.	74LS05	1	BAS	
U5	I.C.	74LS04	1	BAS	
U6	I.C.	MC68008	1	BAS	
U7	I.C.	74LS640	1	BAS	
U8, 9	I.C.	74LS541	2	BAS	
U10, 11	I.C.	74LS367	2	BAS	
U12	I.C.	74LS20	1	BAS	
U13	I.C.	74S571	1	BAS	
U14	I.C.	74LS73	1	BAS	
U15	I.C.	MC68681	1	BAS	
U16	I.C.	74LS164	1	BAS	
U17	I.C.	74LS38	1	BAS	
Y1	Crystal	8 mHz	1	Nymph	NCT050C
Y2	Crystal	3.6864 mHz	1	Nymph	NMP037
- -	Tie wrap (for Y2)	3-7/8"	1	SEA	25-369
J1	Connector (header)	40 pin (20 dbl row)	1	AP Prod.	929836-01



REFERENCE DESIGNATOR CHART

REF. DESIG.	LAST	NOT
C	C22	
J	J1	
R	R6	
RN	RN2	
U	U17	
Y	Y2	

NOTES:
1) FOR PARTS LIST SEE PL-2190
2) FOR SCHEMATIC SEE DS-2190
3) ALL RESISTORS = 1/4W, ±10% TOL
4) C3 THRU C22 = 0.1UF, 50V

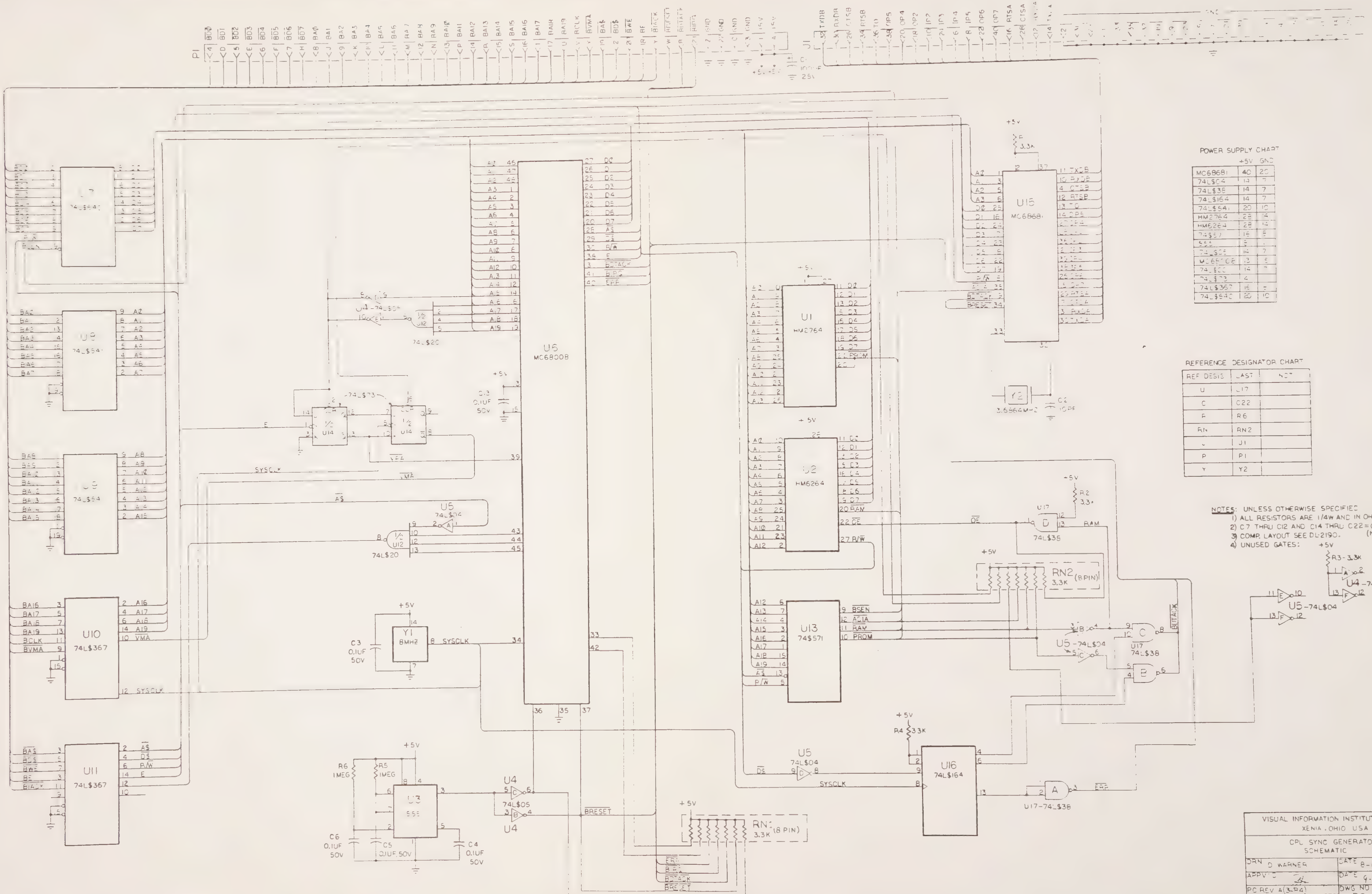
P1

CONDUCTOR SIDE PIN	FUNCTION	COMPONENT SIDE PIN	FUNCTION
A	+5V	1	+5V
B	BDTACK	2	BD6
C	GND	3	GND
D	BD1	4	BD0
E	BD3	5	BD2
F	BD5	6	BD4
H	BD7	7	BD6
J	BA1	8	BA0
K	BA3	9	BA2
L	BA5	10	BA4
M	BA7	11	BA6
N	BA9	12	BA8
P	BA11	13	BA10
R	BA13	14	BA12
S	BA15	15	BA14
T	BA17	16	BA16
U	BA19	17	BA18
V	BCLK	18	BE
W	BRESET	19	BAS
X	BWMA	20	BWE
Y	BTACK	21	BIRQ
Z	GND	22	GND

VISUAL INFORMATION INSTITUTE, INC
XENIA, OHIO

CPU SYNC GENERATOR
COMPONENT LAYOUT

DRN WARNER	DATE 11-8-84
APPV'D	DATE 9-22-85
PC ART REV. A (2-84)	DWG. NO. DL-2190
REV.	



POWER SUPPLY CHART

	+5V	GND
MC68681	40	20
74LS04	14	7
74LS38	14	7
74LS164	14	7
74LS541	20	10
HM2764	28	14
HM6264	28	14
74S57[illegible]	16	8
555	8	1
74LS05	14	7
MC68008	13	5
74LS20	14	7
74LS73	4	
74LS367	16	8
74LS540	20	10

REFERENCE DESIGNATOR CHART

REF DESIG	LAST	NOT
U	U17	
C	C22	
R	R6	
RN	RN2	
J	J1	
P	P1	
Y	Y2	

NOTES: UNLESS OTHERWISE SPECIFIED

1) ALL RESISTORS ARE 1/4W AND IN OHMS 10%.
2) C7 THRU C12 AND C14 THRU C22 = 0.1UF, 50V. (NOT SHOWN).
3) COMP. LAYOUT SEE DL-2190.
4) UNUSED GATES:

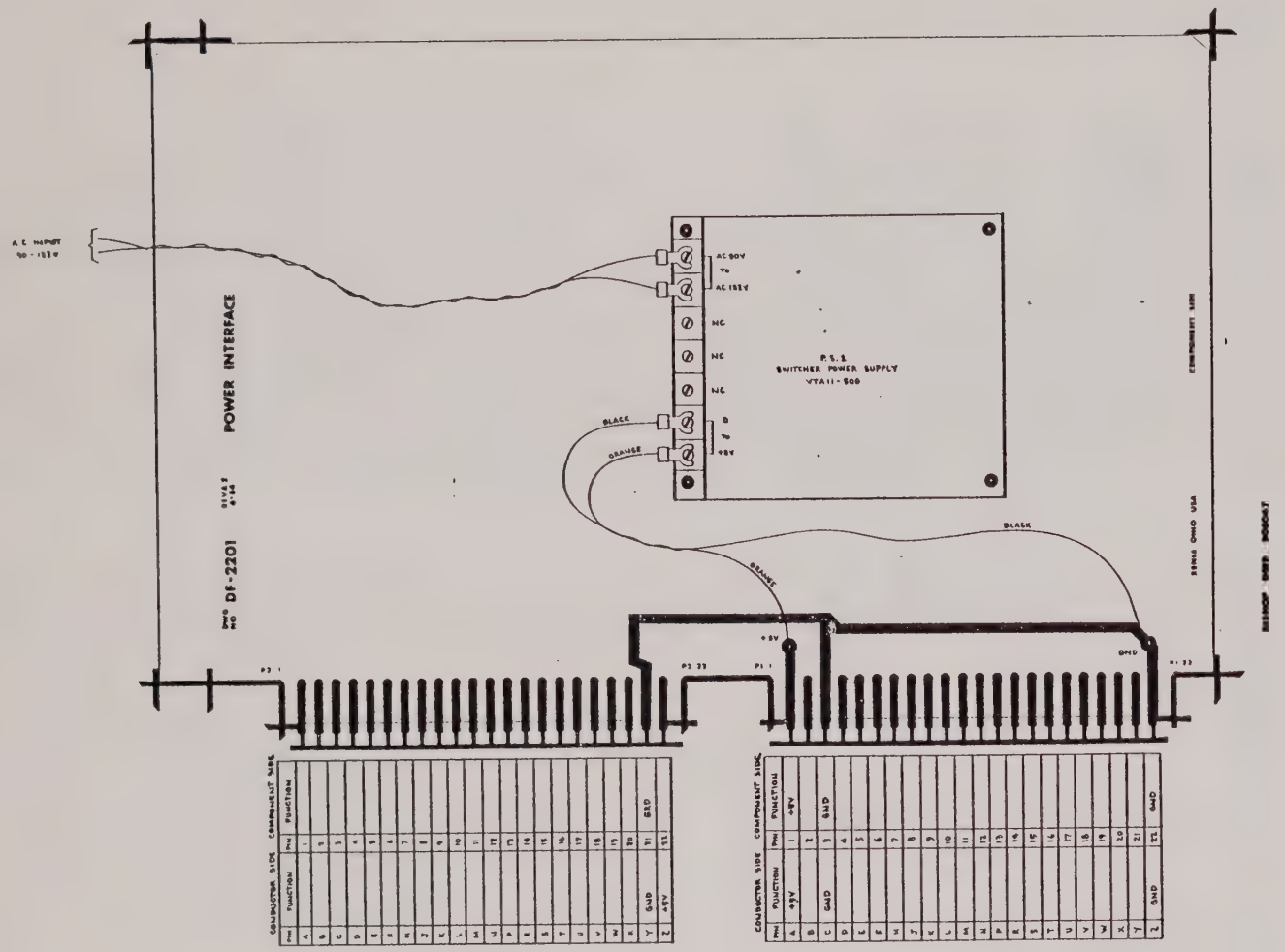
VISUAL INFORMATION INSTITUTE, INC XENIA, OHIO USA	
CPL SYNC GENERATOR SCHEMATIC	
DRN D WARNER	DATE 8-14-84
APPV'D [illegible]	DATE 9-20-84
PC REV A(3-84)	DWG NO
REV 11-5-84	DS-2190

POWER INTERFACE
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-2201

ARTWORK REV. A (6/84) 12/8/84 SHT 1 OF 1

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/ TYPE	QTY	MFR	Vii DWG.NO.
REF.	SCHEMATIC		x	Vii	DS-NONE
REF.	COMPONENT LAYOUT (ASS'Y)		x	Vii	DL-2201
REF.	PC ARTWORK (COND. SIDE)		x	Vii	DB-2201
REF.	PC ARTWORK (COMP. SIDE)		x	Vii	DF-2201
REF.	DRILL DWG.		x	Vii	DD-2201
P.S.1	Switcher, Power Supply	VTA11-500	1	BAS	
—	Solderless Terminals	C63206	4	BAS	



VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
POWER INTERFACE COMPONENT LAYOUT	
DWN PAT ANTONICK	DATE 12-8-84
APPV'D [illegible]	DATE 12-15-84
P.C. ART REV A (6-84)	DWG NO. DL-2201
REV	

MBA PROGRAMMABLE SYNC
PRINTED CIRCUIT BOARD ASSEMBLY

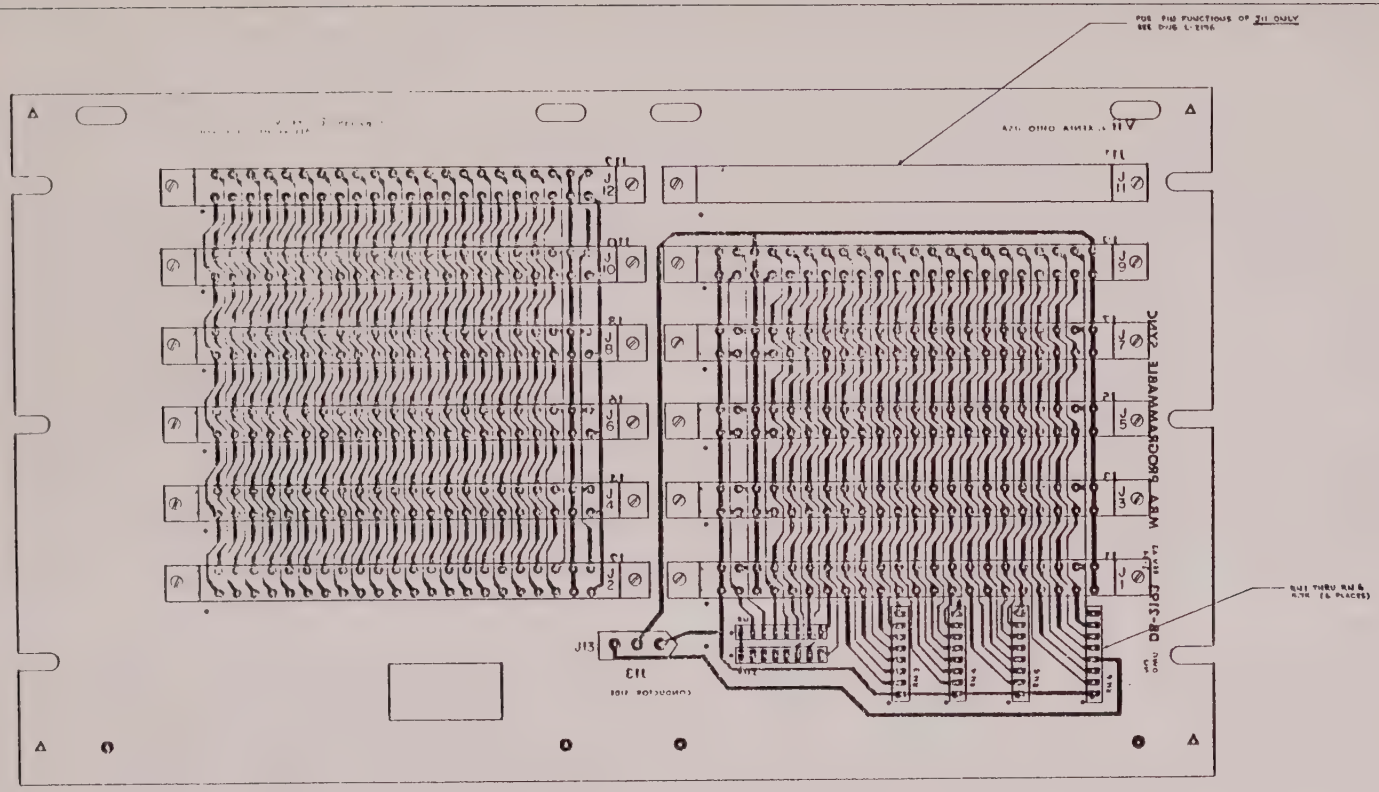
PL-2193

PARTS LIST

SHT 1 OF 1

ARTWORK REV. A (2/84) 1/16/85

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/ TYPE	QTY	MFR	Vii DWG.NO.
REF.	SCHEMATIC			Vii	DS-NONE
REF.	COMPONENT LAYOUT (ASS'Y)			Vii	DL-2193
REF.	PC ARTWORK (COND. SIDE)			Vii	DB-2193
REF.	PC ARTWORK (COMP. SIDE)			Vii	DF-NONE
RN1 - RN6	Resistor Network	4.7K ohm (8 pin)	6	BAS	A-1450
J1, J2	NOT USED		--		
J3-J10,J12	Connector (6266-1)	ESM 22 DRXH	9	Sullins	
J11	Connector (7180-1A)	ESM 22 DREH	1	Sullins	
- -	Screw, pan head	#4-40 x 5/8 lg	24	BAS	
- -	Nut	#4-40	24	BAS	
- -	Lock washer	#4	24	BAS	



REFERENCE DESIGNATOR CHART

REF DESIG.	LAST	NOT
RN	RN 6	
J	J13	

NOTES:
1) FOR PARTS LIST SEE PL-2193.

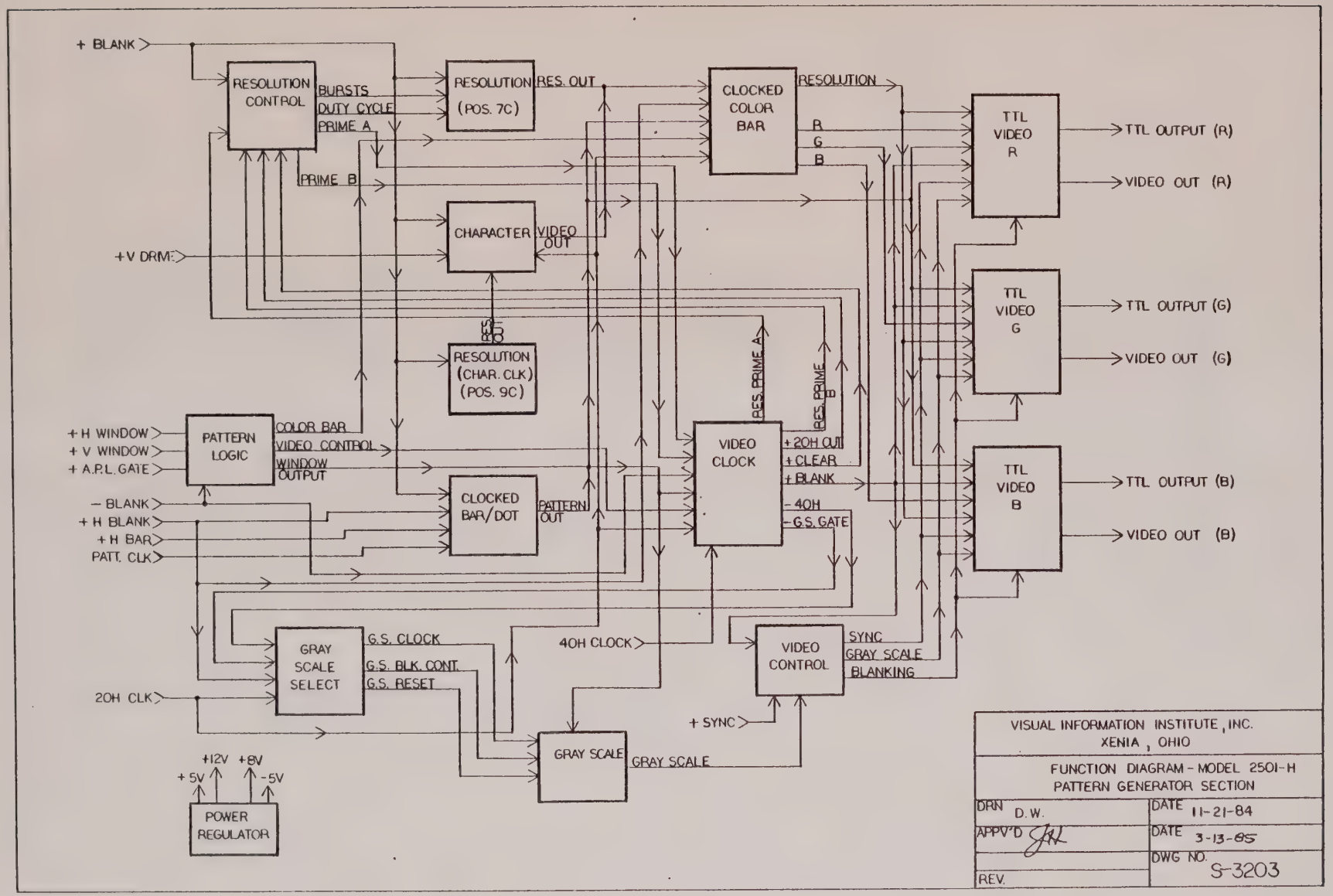
P2

CONDUCTOR SIDE PIN	FUNCTION	COMPONENT SIDE PIN	FUNCTION
A	2H CLK	1	INT H.O.IN
B	BLANK	2	EXT. H.O.IN
C	V SYNC	3	CHAR CONT
D	SYNC	4	PAST CLK
E	2H EQU	5	H GATE
F	H BLANK	6	H WINDOW
H	2H SERR	7	
J	H SYNC	8	
K	V TRIG	9	H DRIVE
L	HEN	10	
M	V TRIG	11	SOURCE
N	V DRIVE	12	MISC.
P	V GATE	13	MISC.
R	H CRYSTAL	14	EXT.
S	V WINDOW	15	
T	V BLANK	16	
U	APL	17	
V	H BAR	18	
W	VB CLK	19	
X		20	CHAR CLK
Y	GND	21	GND
Z	+5V	22	+5V

P1

CONDUCTOR SIDE PIN	FUNCTION	COMPONENT SIDE PIN	FUNCTION
A	+5V	1	+5V
B	SDTACK	2	SD5
C	GND	3	GND
D	SD1	4	SD0
E	SD3	5	SD2
F	SD5	6	SD4
H	SD7	7	SD6
J	SA1	8	SA0
K	SA3	9	SA2
L	SA5	10	SA4
M	SA7	11	SA6
N	SA9	12	SA8
P	SA11	13	SA10
R	SA13	14	SA12
S	SA15	15	SA14
T	SA17	16	SA16
U	SA19	17	SA18
V	B CLK	18	BE
W	B RESET	19	SA5
X	SYNA	20	SWE
Y	SIACK	21	SIRQ
Z	GND	22	GND

VISUAL INFORMATION INSTITUTE INC XENIA, OHIO USA	
MSA PROGRAMMABLE SYNC COMPONENT LAYOUT	
DWN PAT ANTONICK	DATE 5-16-84
APPD [illegible]	DATE [illegible]
REV. 11-16-85	DWG NO DL-2193
P.C. ART REV	



VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
FUNCTION DIAGRAM - MODEL 2501-H PATTERN GENERATOR SECTION	
DRN D.W.	DATE 11-21-84
APP'D	DATE 3-13-85
REV.	DWG NO. S-3203

VIDEO CONTROL
PRINTED CIRCUIT BOARD ASSEMBLY

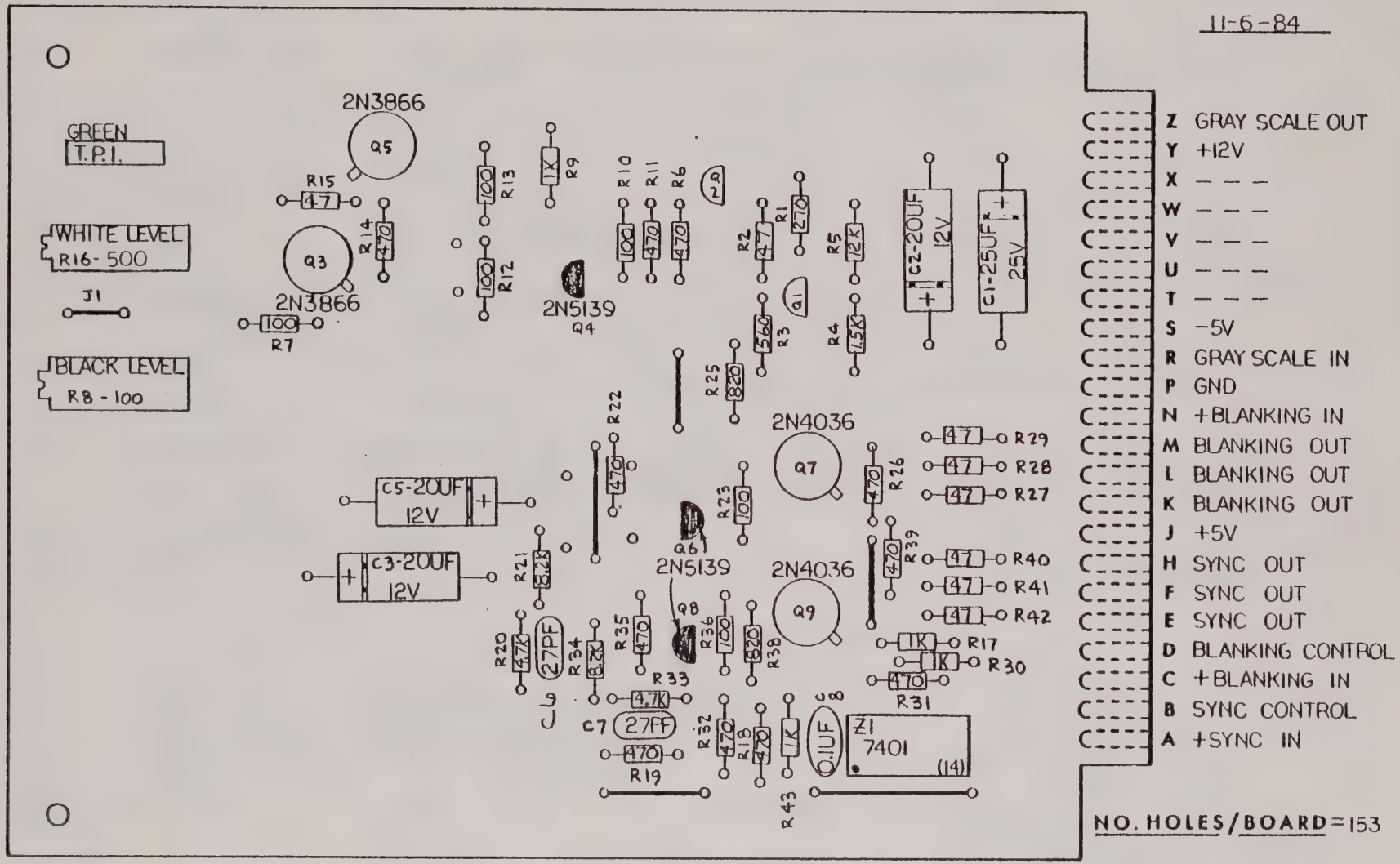
PARTS LIST PL-4010

ARTWORK REV. A (8/84) 11/6/84 SHT 1 OF 1

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	MFR.	Vii DWG.NO.
PCB ASSEMBLY		x	Vii	L-4010
PCB ARTWORK	COND. SIDE	x	Vii	CB-4010
PCB ARTWORK	COMP. SIDE	x	Vii	CF-NONE
PCB SCHEMATIC		x	Vii	S-4010
Hole Count		153		
Transistors	2N5134	2	BAS	A-1844
"	2N5139	3	BAS	A-1845
"	2N3866	2	BAS	A-1859
"	2N4036	2	BAS	A-1862
Resistor, Fixed	47 ohms	8	BAS	A-1450
"	100 ohms	6	BAS	A-1450
"	270 ohms	1	BAS	A-1450
"	470 ohms	11	BAS	A-1450
"	560 ohms	1	BAS	A-1450
"	820 ohms	2	BAS	A-1450
"	1K ohms	4	BAS	A-1450
"	1.5K ohms	1	BAS	A-1450
"	4.7K ohms	2	BAS	A-1450
"	8.2K ohms	2	BAS	A-1450
"	12K ohms	1	BAS	A-1450
Resistor, Var.	100 ohms	1	BAS	A-1460
"	500 ohms	1	BAS	A-1460
Capacitor	27 pf	2	BAS	A-1454
"	0.1 uf, 10v	1	BAS	A-1455
"	20 uf, 12v	3	BAS	A-1458
"	25 uf, 25v	1	BAS	A-1458
I.C. Socket	14 pin	1	BAS	A-1465
I.C.	7401	1	BAS	
Test Point	Green (P.C.)	1	BAS	A-1766
Jumper, Bus Wire	#22 Awg Solid	6	BAS	

VIDEO CONTROL REV. A (8-84) DWG. NO. L-4010 (GROUP I)

PARTS LIST
11-6-84



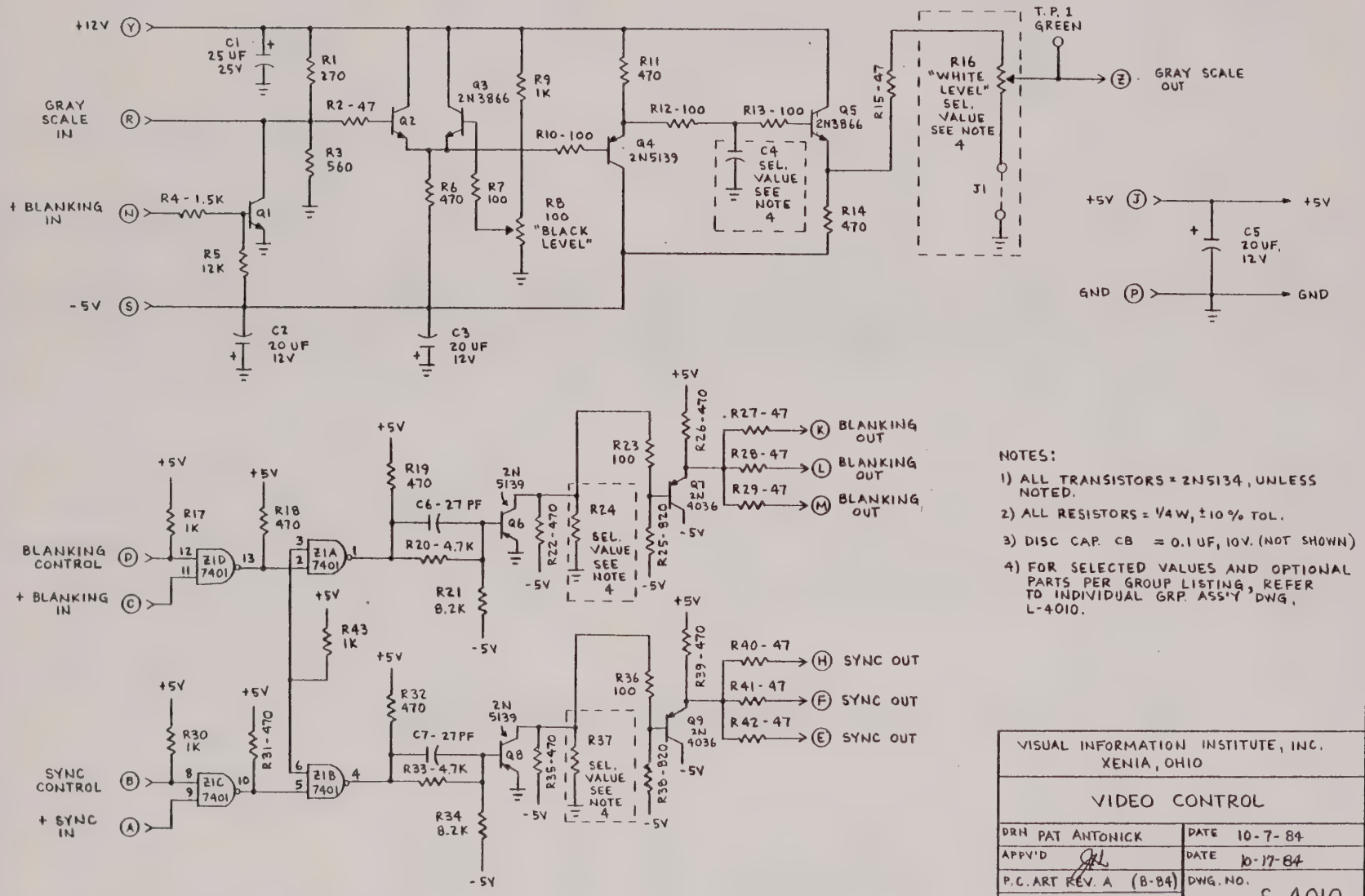
NO. HOLES/BOARD = 153

NOTES:
1) RESISTORS = 1/4W; ±10% TOL.
2) TRANSISTORS = 2N5134 UNLESS NOTED.
3) o—o = BUS WIRE JUMPER. #22 AWG SOLID.

POSITION 3B 4010 VIDEO CONTROL (Group 1)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	GRAY SCALE OUT . .	(TTL VIDEO (3C,4C,5C), PIN K)
Y	+12v.	(+12v. BUSS)(POWER REGULATOR, PIN Y)
X	--	
W	--	
V	--	
U	--	
T	--	
S	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
R	GRAY SCALE IN . .	(GRAY SCALE, PIN A)
P	GROUND	(GROUND BUSS)
N	+BLANK IN	(VIDEO CONTROL, PIN C)(VIDEO CLOCK, PIN C)(TTL VIDEO (3C,4C,5C), PIN S)
M	--	
L	-BLANK OUT	(TTL VIDEO (3C,4C,5C), PIN C)
K	--	
J	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
H	--	
F	-SYNC OUT	(TTL VIDEO (3C,4C,5C), PIN A)
E	--	
D	--	
C	+BLANK IN	(VIDEO CONTROL, PIN N)(VIDEO CLOCK, PIN C)(TTL VIDEO (3C,4C,5C), PIN S)
B	--	
A	+SYNC IN	(PULSE OUTPUT, PIN E)(TTL PULSE OUTPUT, PIN E) (uP INTERFACE (P1), PIN 3)
	GROUND	(TTL VIDEO (3C), GROUND)



NOTES:

1) ALL TRANSISTORS = 2N5134, UNLESS NOTED.
2) ALL RESISTORS = 1/4 W, ±10 % TOL.
3) DISC CAP. CB = 0.1 UF, 10V. (NOT SHOWN)
4) FOR SELECTED VALUES AND OPTIONAL PARTS PER GROUP LISTING, REFER TO INDIVIDUAL GRP. ASS'Y DWG, L-4010.

VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
VIDEO CONTROL	
DRN PAT ANTONICK	DATE 10-7-84
APP'D	DATE 10-17-84
P.C. ART REV. A (8-84)	DWG. NO. S-4010
REV. 11-6-84	

GRAY SCALE
PRINTED CIRCUIT BOARD ASSEMBLY

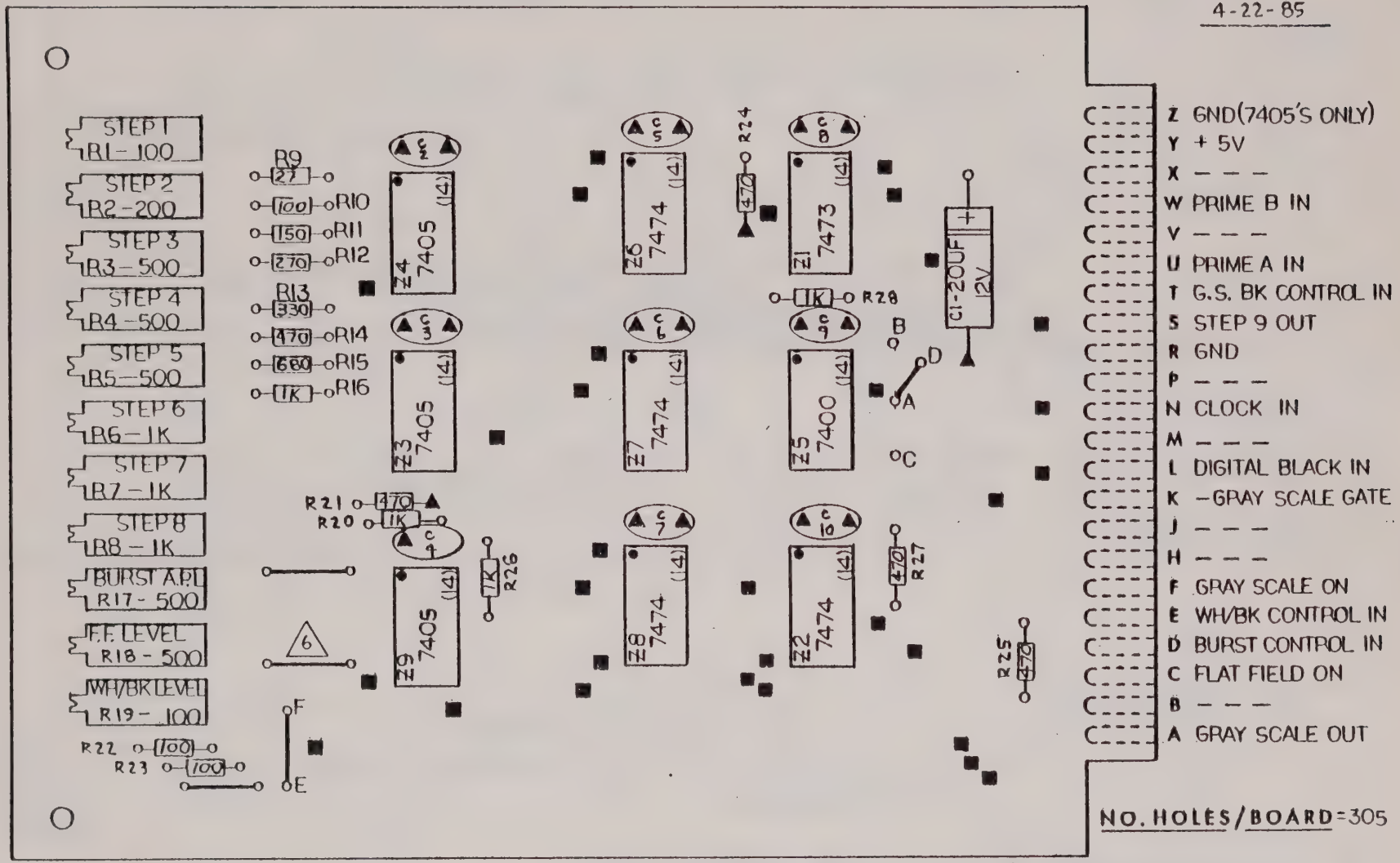
PARTS LIST PL-4000

ARTWORK REV. B (10/84) 10/10/84 SHT 1 OF 1

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	QTY/GROUP 2	MFR.	Vii DWG.NO.
PCB ASSEMBLY		x	x	Vii	L-4000
PCB ARTWORK	COND. SIDE	x	x	Vii	CB-4000
PCB ARTWORK	COMP. SIDE	x	x	Vii	CF-4000
PCB SCHEMATIC		x	x	Vii	S-4000
Hole Count		300	305		
Resistor, Fixed	27 ohms	1	1	BAS	A-1450
	100 ohms	2	3	BAS	A-1450
"	150 ohms	1	1	BAS	A-1450
"	270 ohms	1	1	BAS	A-1450
"	330 ohms	1	1	BAS	A-1450
"	470 ohms	5	5	BAS	A-1450
"	680 ohms	1	1	BAS	A-1450
"	1K ohms	4	4	BAS	A-1450
Resistor, Var.	100 ohms	2	2	BAS	A-1460
"	200 ohms	1	1	BAS	A-1460
"	500 ohms	4	5	BAS	A-1460
"	1K ohms	3	3	BAS	A-1460
Capacitor	20uf, 12v	1	1	BAS	A-1458
"	0.1uf, 10v	9	9	BAS	A-1455
I.C. Socket	14 pin	9	9	BAS	A-1465
I.C.	7400	1	1	BAS	A-1747
"	7405	3	3	BAS	A-1754
"	7473	1	1	BAS	A-1756
"	7474	4	4	BAS	
Bus Wire, Jumper	#22 Awg, Solid	5	5	BAS	
Comp Feed Thru = ▲		20	20		
Wire Feed Thru = ■	#22 Awg, Solid	31	31		

GRAY SCALE REV.B (10-84) DWG. NO. L-4000 (GROUP 2)

PARTS LIST
4-22-85



NO. HOLES/BOARD=305

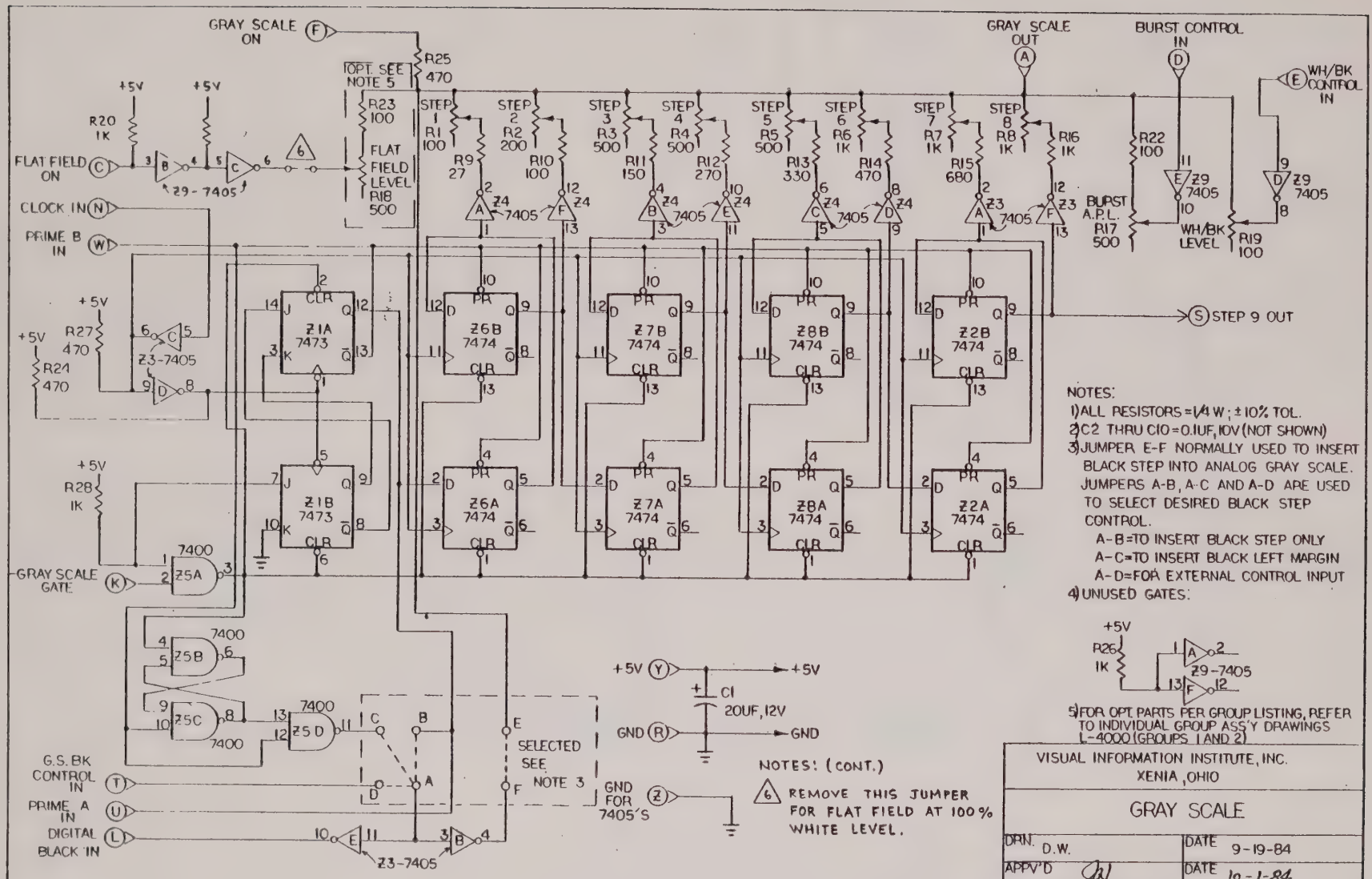
NOTES: 1) ALL RESISTORS = 1/4 W; ±10% TOL.
2) C2 THRU C10 = 0.1UF, 10V
3) o——o = BUS WIRE *22AWG, SOLID
4) SOLDER ON BOTH SIDES OF P.C. BOARD:
▲ = COMP. FEED THRU.
■ = WIRE FEED THRU; *22AWG, SOLID
5) JUMPER E-F NORMALLY USED TO INSERT BLACK STEP INTO ANALOG GRAY SCALE. JUMPERS A-B, A-C AND A-D ARE USED TO SELECT DESIRED BLACK STEP CONTROL.
A-B = TO INSERT BLACK STEP ONLY
A-C = TO INSERT BLACK LEFT MARGIN
A-D = FOR EXTERNAL CONTROL INPUT

6 REMOVE THIS JUMPER FOR FLAT FIELD LEVEL AT 100% WHITE.

POSITION 4B 4000 GRAY SCALE (Group 2)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Ƶ	GRAY SCALE GROUND .	(GROUND BUSS)
Y	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
X	--	
W	--	
V	--	
U	PRIME A IN	(GRAY SCALE SELECT, PIN Ƶ)
T	GS BLACK CONTROL .	(GRAY SCALE SELECT, PIN J)
S	--	
R	GROUND	(GROUND BUSS)
P	--	
N	CLOCK IN	(GRAY SCALE SELECT, PIN U)
M	--	
L	DIGITAL BLACK IN .	(TTL VIDEO (3C,4C,5C), PIN P)(CLOCKED COLOR BAR, PIN B)(VIDEO CLOCK, PIN R) (CLOCKED BAR/DOT, PIN U)(PATTERN LOGIC, PIN Ƶ)
K	-GS GATE IN	(GRAY SCALE SELECT, PIN Y)
J	--	
H	--	
F	--	
E	WH/BL CONTROL IN .	(VIDEO CLOCK, PIN A)
D	BURST CONTROL . . .	(RESOLUTION CONTROL, PIN Ƶ)
C	FLAT FIELD ON . . .	(CONTROL PANEL, S3, FUNCTION SELECT - FLAT FIELD)
B	--	
A	GRAY SCALE	(VIDEO CONTROL, PIN R)



NOTES:

1) ALL RESISTORS = 1/4 W; ± 10% TOL.
2) C2 THRU C10 = 0.1UF, 10V (NOT SHOWN)
3) JUMPER E-F NORMALLY USED TO INSERT BLACK STEP INTO ANALOG GRAY SCALE. JUMPERS A-B, A-C AND A-D ARE USED TO SELECT DESIRED BLACK STEP CONTROL.
   - A-B = TO INSERT BLACK STEP ONLY
   - A-C = TO INSERT BLACK LEFT MARGIN
   - A-D = FOR EXTERNAL CONTROL INPUT
4) UNUSED GATES:

5) FOR OPT. PARTS PER GROUP LISTING, REFER TO INDIVIDUAL GROUP ASS'Y DRAWINGS L-4000 (GROUPS 1 AND 2)

NOTES: (CONT.)

6 REMOVE THIS JUMPER FOR FLAT FIELD AT 100% WHITE LEVEL.

VISUAL INFORMATION INSTITUTE, INC.
XENIA, OHIO

GRAY SCALE

DRN. D.W.	DATE 9-19-84
APPV'D	DATE 10-1-84
P.C. ART REV. B (10-84)	DWG. NO. S-4000
REV. 4-22-85	

GRAY SCALE SELECT
PRINTED CIRCUIT BOARD ASSEMBLY

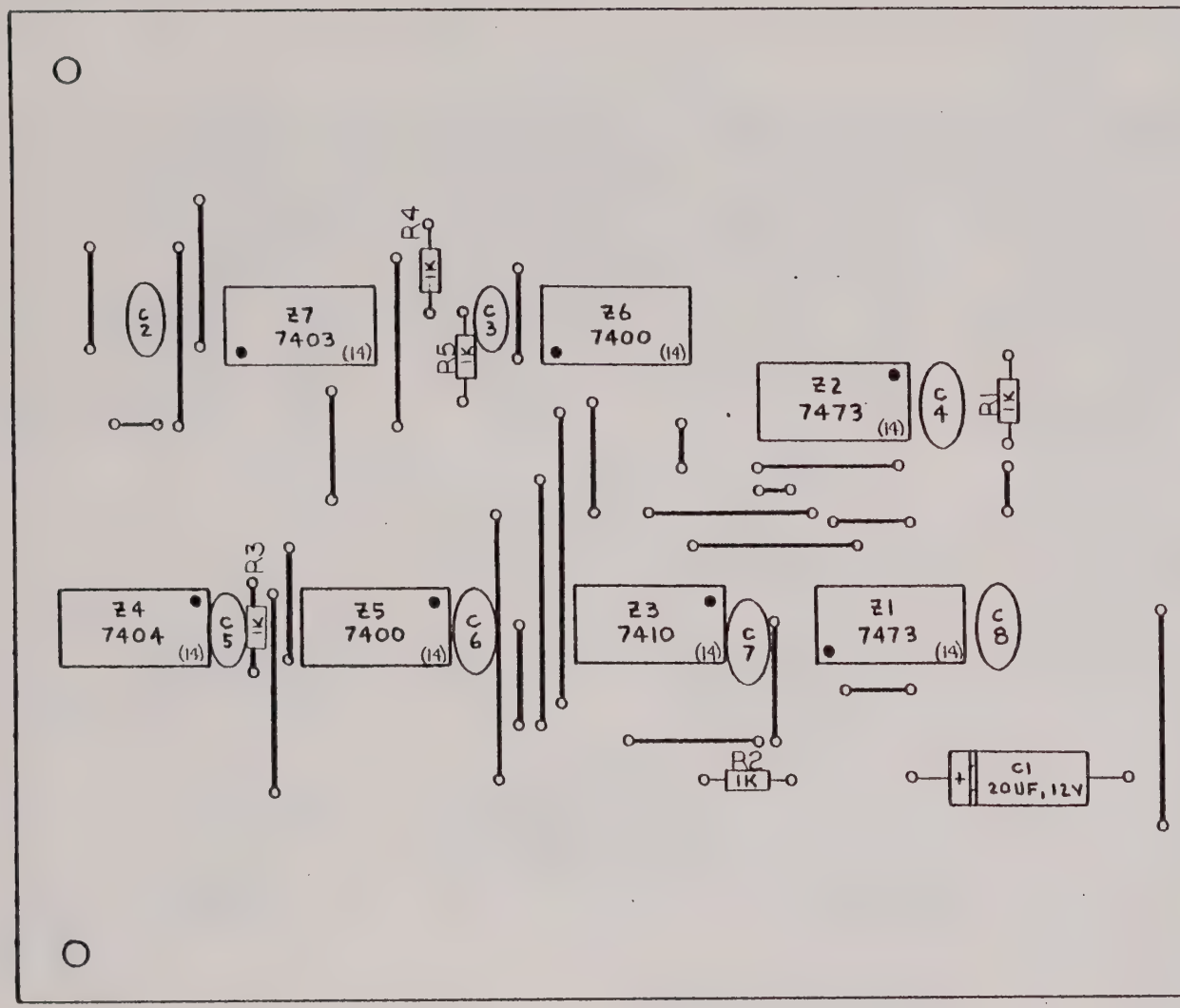
PARTS LIST PL-4007

ARTWORK REV. A (8/84) 10/19/84 SHT 1 OF 1

DESCRIPTION	VALUE/TYPE	QTY/GROUP 0	MFR.	Vii DWG.NO.
PCB ASSEMBLY		x	Vii	L-4007
PCB ARTWORK	COND. SIDE	x	Vii	CB-4007
PCB ARTWORK	COMP. SIDE	x	Vii	CF-NONE
PCB SCHEMATIC		x	Vii	S-4007
Hole Count		174		
Resistor, Fixed	1K ohms	5	BAS	A-1450
Capacitor	0.1uf, 10v.	7	BAS	A-1455
Capacitor	20uf, 12v	1	BAS	A-1458
I.C. Socket	14 pin	7	BAS	A-1465
I.C.	7400	2	BAS	A-1747
"	7403	1	BAS	A-1748
"	7404	1	BAS	
"	7410	1	BAS	
"	7473	2	BAS	A-1756
Bus wire, jumper	#22 Awg Solid	25	BAS	

GRAY SCALE SELECT B-84 REV. A DWG. NO. L-4007 (GROUP O)

PARTS LIST
10-19-84



Z	PRIME A IN
Y	G.S. RESET OUT
X	40H CLOCK IN
W	---
V	---
U	G.S. CLOCK OUT
T	---
S	---
R	---
P	---
N	---
M	---
L	---
K	GND
J	G.S. BLK CONT. OUT
H	+5V
F	G.S. ON
E	20H CLOCK IN
D	+H GATE IN
C	G.S. GATE IN
B	---
A	---

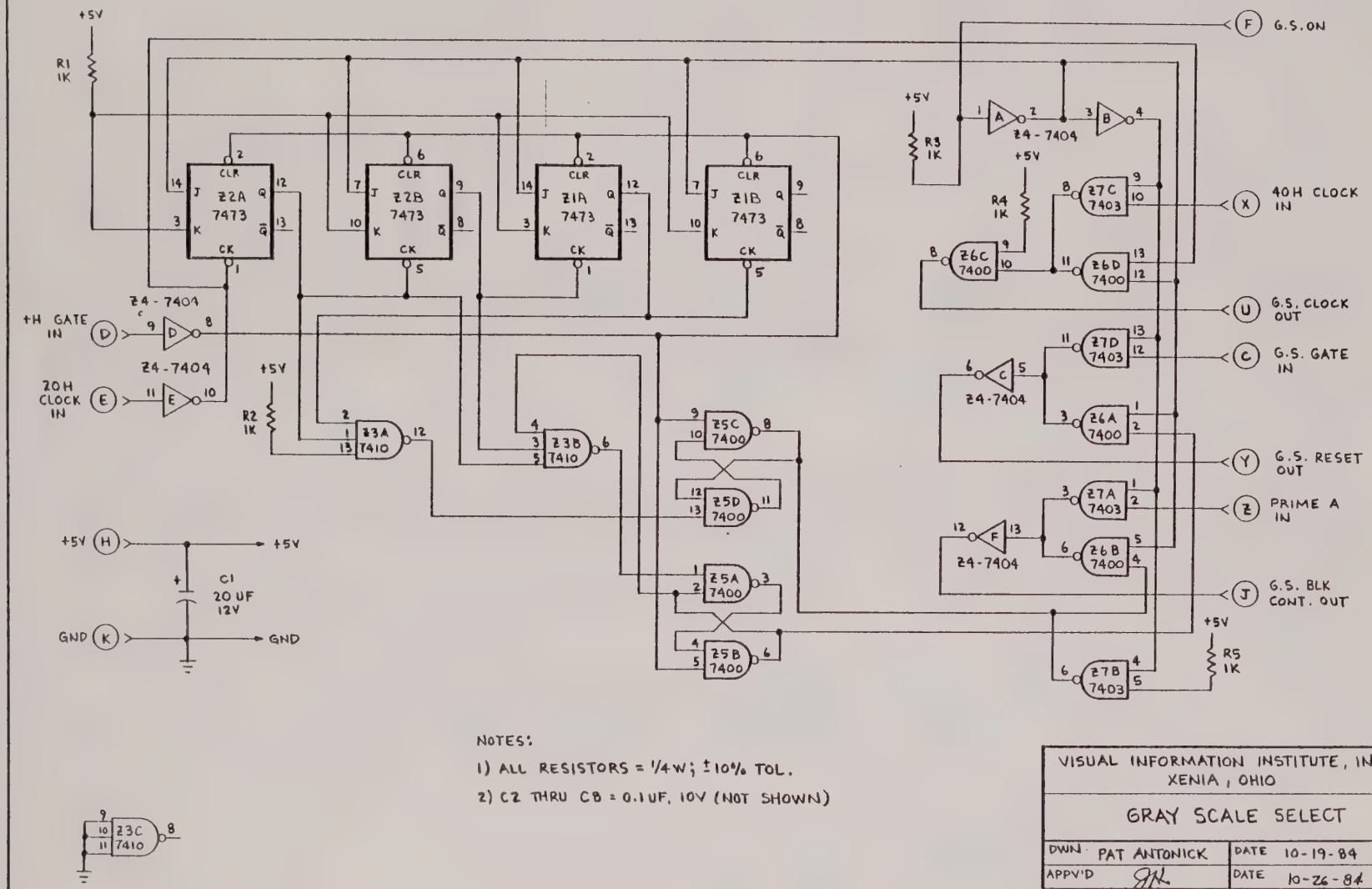
NO. HOLES/BOARD=174

NOTES:
1) ALL RESISTORS = 1/4W, ±10% TOL.
2) C2 THRU C8 = 0.1UF, 10V
3) o—o = BUS WIRE, #22AWG, SOLID

POSITION 5B 4007 GRAY SCALE SELECT (Group 0)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	PRIME A IN	(GRAY SCALE, PIN U)
Y	GS GATE OUT	(GRAY SCALE, PIN K)
X	-40H CLOCK IN . . .	(VIDEO CLOCK, PIN Z)
W	--	
V	--	
U	GS CLOCK OUT . . .	(GRAY SCALE, PIN N)
T	--	
S	--	
R	--	
P	--	
N	--	
M	--	
L	--	
K	GROUND	(GROUND BUSS)
J	GS BLACK CONTROL .	(GRAY SCALE, PIN T)
H	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
F	GRAY SCALE ON . . .	(CONTROL PANEL, S3, FUNCTION SELECT - GRAY SCALE)
E	-20H CLOCK IN . . .	(CLOCKED COLOR BAR, PIN H)(uP INTERFACE (P1), PIN R)
D	+H BLANK IN	(VIDEO CLOCK, PIN F)(CLOCKED BAR/DOT, PIN D)(uP INTERFACE (P1), PIN 4) (CLOCKED COLOR BAR, PIN J)(CHARACTER, PIN X)
C	-GS GATE IN	(VIDEO CLOCK, PIN T)
B	--	
A	--	



NOTES:

1) ALL RESISTORS = 1/4 W; ±10% TOL.

2) C2 THRU C8 = 0.1 UF, 10V (NOT SHOWN)

VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
GRAY SCALE SELECT	
DWN: PAT ANTONICK	DATE 10-19-84
APPV'D	DATE 10-26-84
P.C. ART REV. A (8-84)	DWG. NO. S-4007
REV	

VIDEO CLOCK
PRINTED CIRCUIT BOARD ASSEMBLY

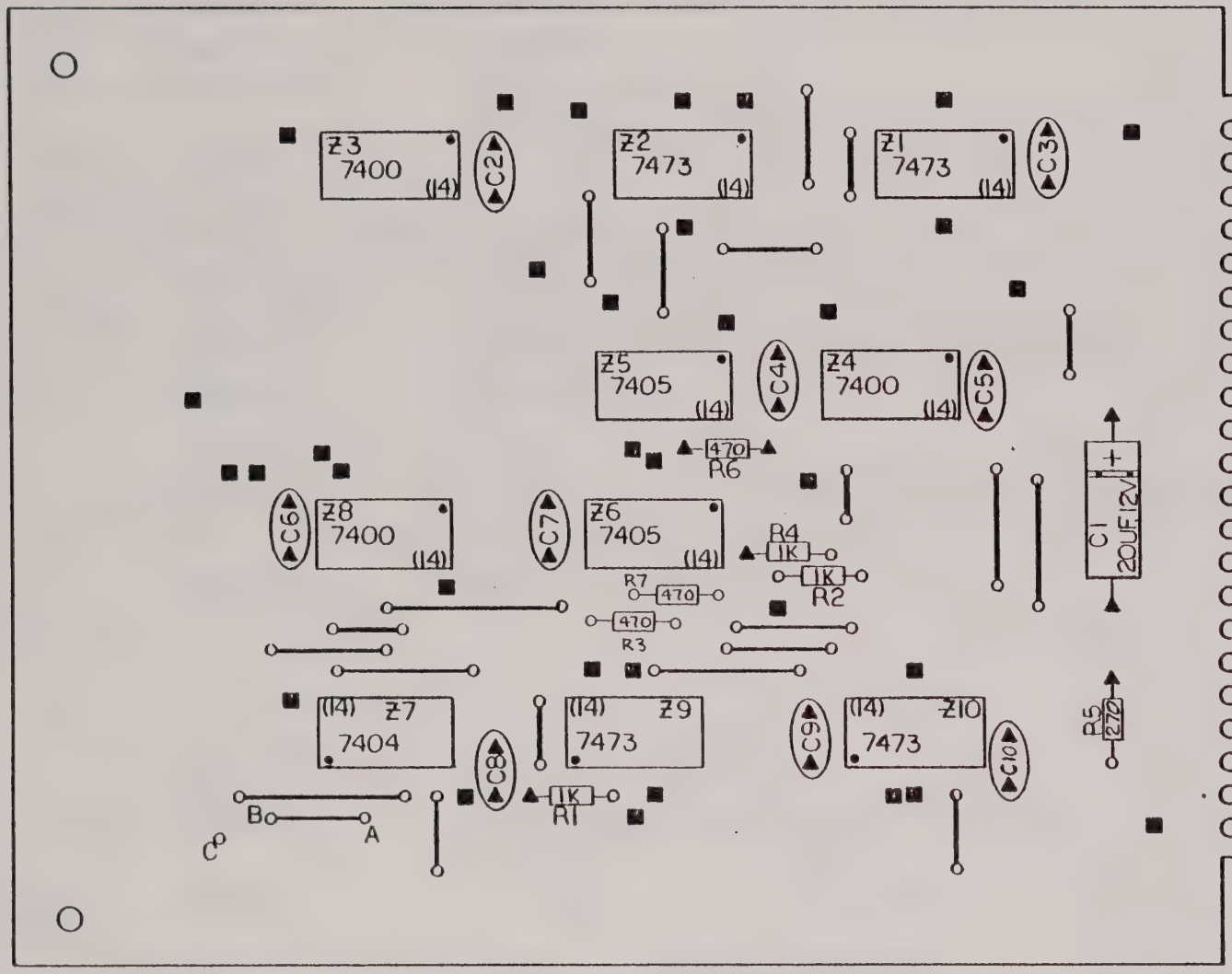
PARTS LIST PL-4001

ARTWORK REV. B (3/85) 3/6/85 SHT 1 of 1

DESCRIPTION	VALUE/TYPE	QTY/GROUP 0	MFR.	Vii DWG.NO.
PCB ASSEMBLY		X	Vii	L-4001
PCB ARTWORK	COND. SIDE	X	Vii	CB-4001
PCB ARTWORK	COMP. SIDE	X	Vii	CF-4001
PCB SCHEMATIC			Vii	S-4001
Hole Count		307		
Resistor, Fixed	1K ohms	3	BAS	A-1450
"	270 ohms	1	BAS	A-1450
"	470 ohms	3	BAS	A-1450
Capacitor	0.1uf, 10v	9	BAS	A-1455
"	20uf, 12v	1	BAS	A-1458
I.C. Socket	14 pin	10	BAS	A-1465
I.C.	7400	3	BAS	A-1747
"	7404	1	BAS	
"	7405	2	BAS	A-1754
"	7473	4	BAS	A-1756
Bus wire, jumper	#22 Awg Solid	20	BAS	
Wire feed thru =■	#22 Awg Solid	34	BAS	
Comp. feed thru =▲		25		

VIDEO CLOCK REV. B (3-85) DWG. NO. L-4001 (GROUP 0)

PARTS LIST
3-6-85



Z -40H OUT
Y PRIME B IN
X PRIME A IN
W PRIME A OUT
V GRAY SCALE IN
U PRIME B OUT
T -G.S. GATE OUT
S +5V
R PATTERN IN
P VIDEO ON(GND)
N +20H OUT
M REF. ON
L RES. PRIME B
K RES. PRIME A
J GND
H -20H OUT
F +H BLANK IN
E +CLEAR OUT
D +40H CLOCK IN
C +BLANK OUT
B -BLANK IN
A WH/BK CONT. OUT

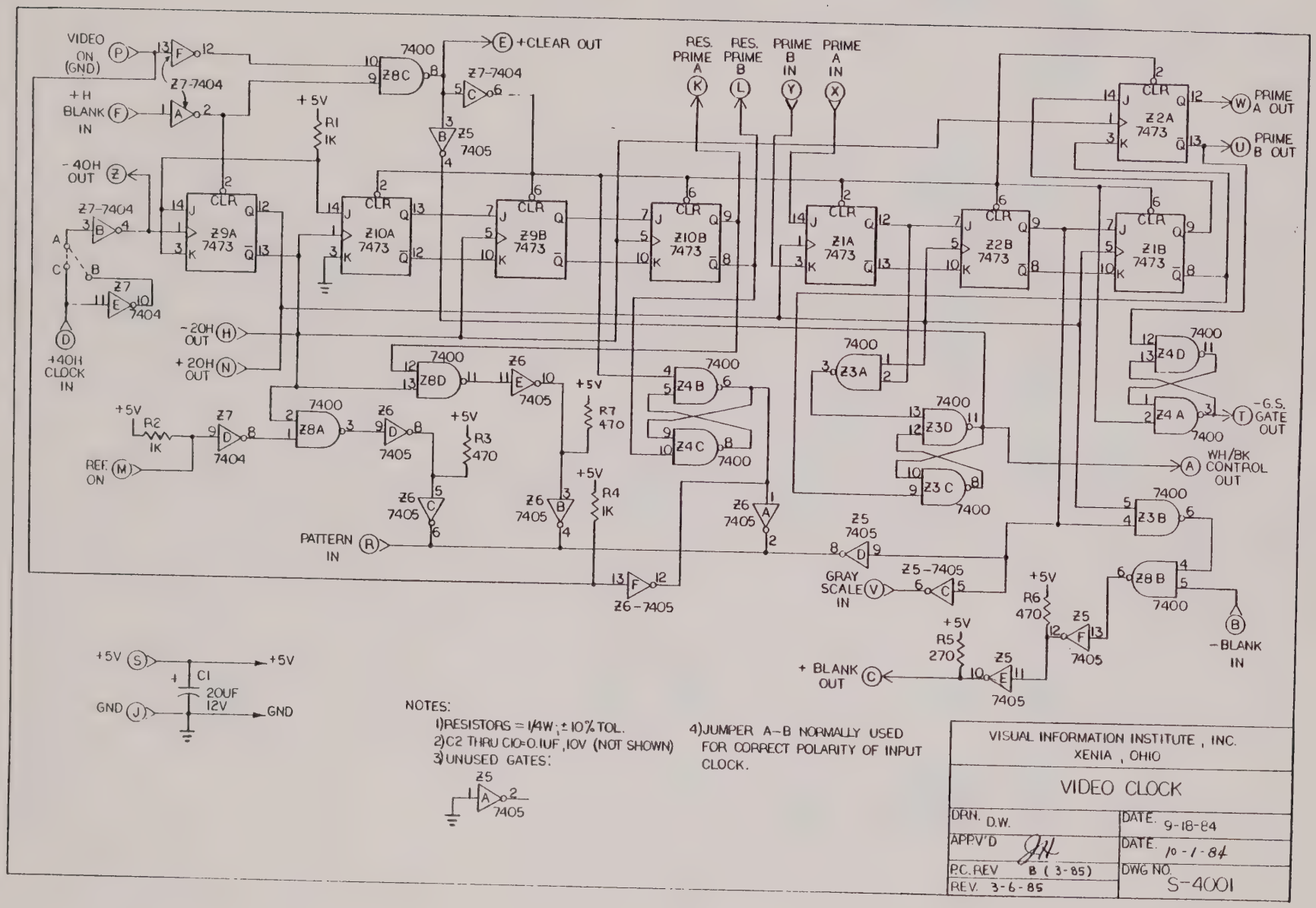
NO. HOLES/BOARD=307

NOTES:
1) RESISTORS=1 4W; ±10% TOL.
2) C2 THRU C10 = 0.1UF, 10V
3) o—o = BUS WIRE JUMPER, #22 AWG SOLID
4) SOLDER BOTH SIDES OF BOARD;
▲=COMP. FEED THRU
■=#22 AWG, WIRE FEED THRU.

POSITION 6B 4001 VIDEO CLOCK (Group 0)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	-40H OUT	(GRAY SCALE SELECT, PIN X)
Y	PRIME B IN	(RESOLUTION CONTROL, PIN D)
X	PRIME A IN	(RESOLUTION CONTROL, PIN B)
W	--	
V	--	
U	--	
T	-GS GATE OUT . . .	(GRAY SCALE SELECT, PIN C)
S	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
R	PATTERN IN	(GRAY SCALE, PIN L)(TTL VIDEO (3C,4C,5C), PIN P)(CLOCKED COLOR BAR, PIN B) (CLOCKED BAR/DOT, PIN U)(PATTERN LOGIC, PIN Z)
P	VIDEO ON	(PATTERN LOGIC, PIN N)
N	+20H OUT	(RESOLUTION CONTROL, PIN X)
M	REF ON	(CONTROL PANEL, S2, RESOLUTION REP RATE - REFERENCE)
L	RES PRIME B . . .	(RESOLUTION CONTROL, PIN V)
K	RES PRIME A . . .	(RESOLUTION CONTROL, PIN U)
J	GROUND	(GROUND BUSS)
H	--	
F	+H BLANK IN . . .	(GRAY SCALE SELECT, PIN D)(CLOCKED COLOR BAR, PIN J)(CHARACTER, PIN X) (CLOCKED BAR/DOT, PIN D)(uP INTERFACE (P1), PIN 4)
E	+CLEAR OUT	(RESOLUTION CONTROL, PIN W)
D	+40H CLOCK IN . .	(uP INTERFACE (P1), PIN C)
C	+BLANK OUT	(VIDEO CONTROL, PINS C, N)(TTL VIDEO (3C,4C,5C), PIN S)
B	-BLANK IN	(PATTERN LOGIC, PIN E)(uP INTERFACE (P1), PIN F)
A	WH/BL CONTROL . .	(GRAY SCALE, PIN E)



NOTES:

1) RESISTORS = 1/4W, ± 10% TOL.
2) C2 THRU C10 = 0.1UF, 10V (NOT SHOWN)
3) UNUSED GATES:

4) JUMPER A–B NORMALLY USED FOR CORRECT POLARITY OF INPUT CLOCK.

VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
VIDEO CLOCK	
DRN. D.W.	DATE. 9-18-84
APPV'D JH	DATE. 10-1-84
P.C. REV B (3-85)	DWG NO. S-4001
REV. 3-6-85	

RESOLUTION CONTROL
PRINTED CIRCUIT BOARD ASSEMBLY

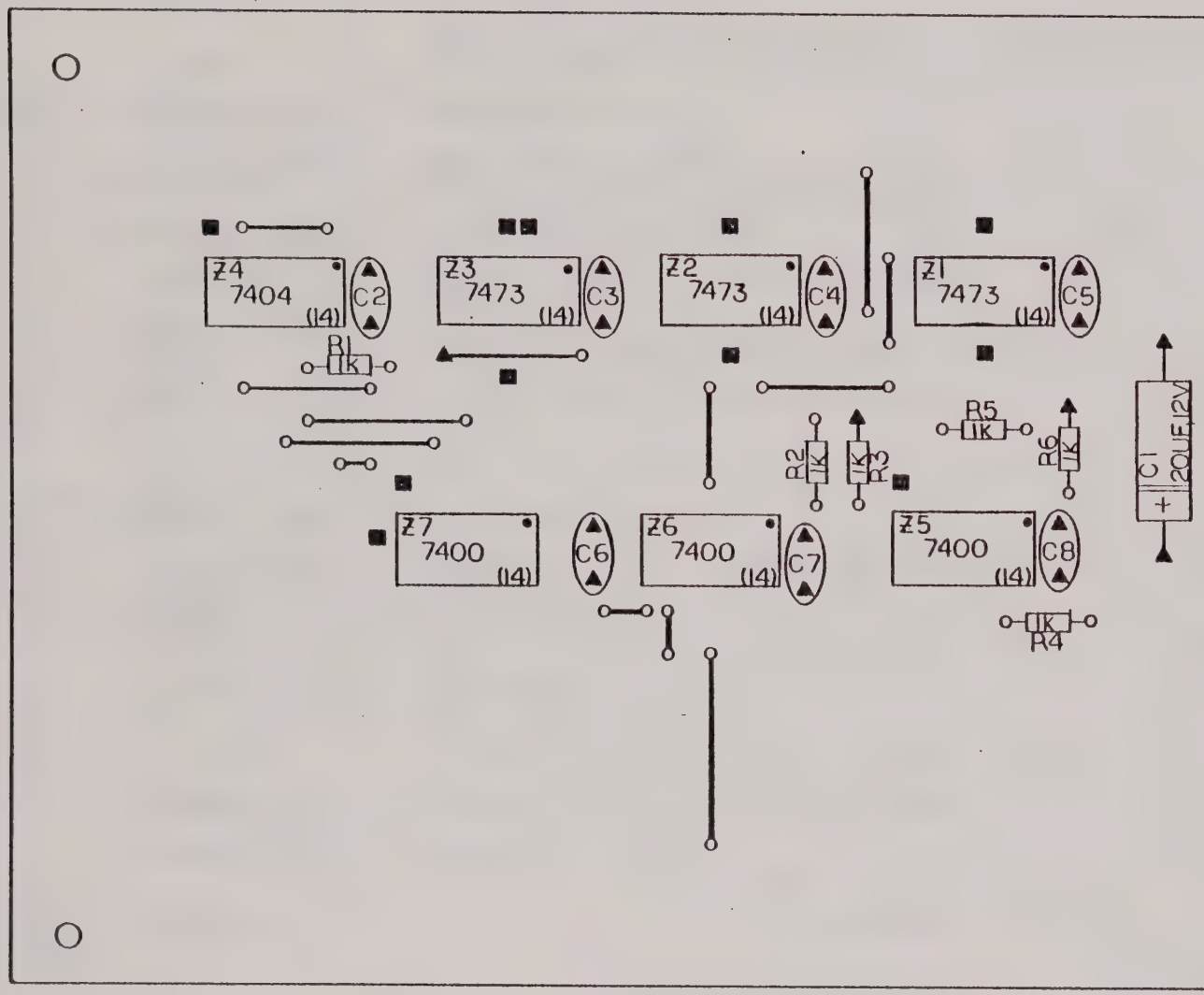
PARTS LIST

PL-4002

ARTWORK REV. A (8/84) 9/21/84 SHT 1 OF 1

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/ TYPE	QTY	MFR	Vii DWG.NO.
REF.	PC ASSEMBLY			Vii	L-4002
REF.	PC ARTWORK (COND. SIDE)			Vii	CB-4002
REF.	PC ARTWORK (COMP. SIDE)			Vii	CF-4002
REF.	SCHEMATIC			Vii	S-4002
R1 thru R6	Resistor, Fixed	1K ohms	6	BAS	A-1450
C1	Capacitor	20uf, 12v	1	BAS	A-1458
C2 thru C8	Capacitor	0.1uf, 10v	7	BAS	A-1455
- -	I.C. Socket	14 pin	7	BAS	A-1465
Z1,2,3	I.C.	7473	3	BAS	A-1756
Z4	I.C.	7404	1	BAS	
Z5,6,7	I.C.	7400	3	BAS	A-1747
- -	Bus wire, jumper	#22 Awg Solid	13	BAS	
- -	Wire feed thru = ■	#22 Awg Solid	11	BAS	
REF.	Comp. feed thru = ▲		19		

RESOLUTION CONTROL REV. A (8-84) DWG. NO. L-4002 (GROUP 0)



PARTS LIST

9-21-84

Z	A.P.L. CONTROL OUT
Y	BURSTS ON
X	+20H CLOCK IN
W	CLEAR IN
V	PRIME B IN
U	PRIME A IN
T	GND
S	BURST 1 ON
R	BURST 1 CONTROL
P	BURST 2 ON
N	BURST 2 CONTROL
M	BURST 3 ON
L	+5V
K	BURST 3 CONTROL
J	BURST 4 ON
H	BURST 4 CONTROL
F	BURST 5 ON
E	BURST 5 CONTROL
D	PRIME B OUT
C	+BLANK IN
B	PRIME A OUT
A	DUTY CYCLE CONTROL

NO. HOLES/BOARD = 193

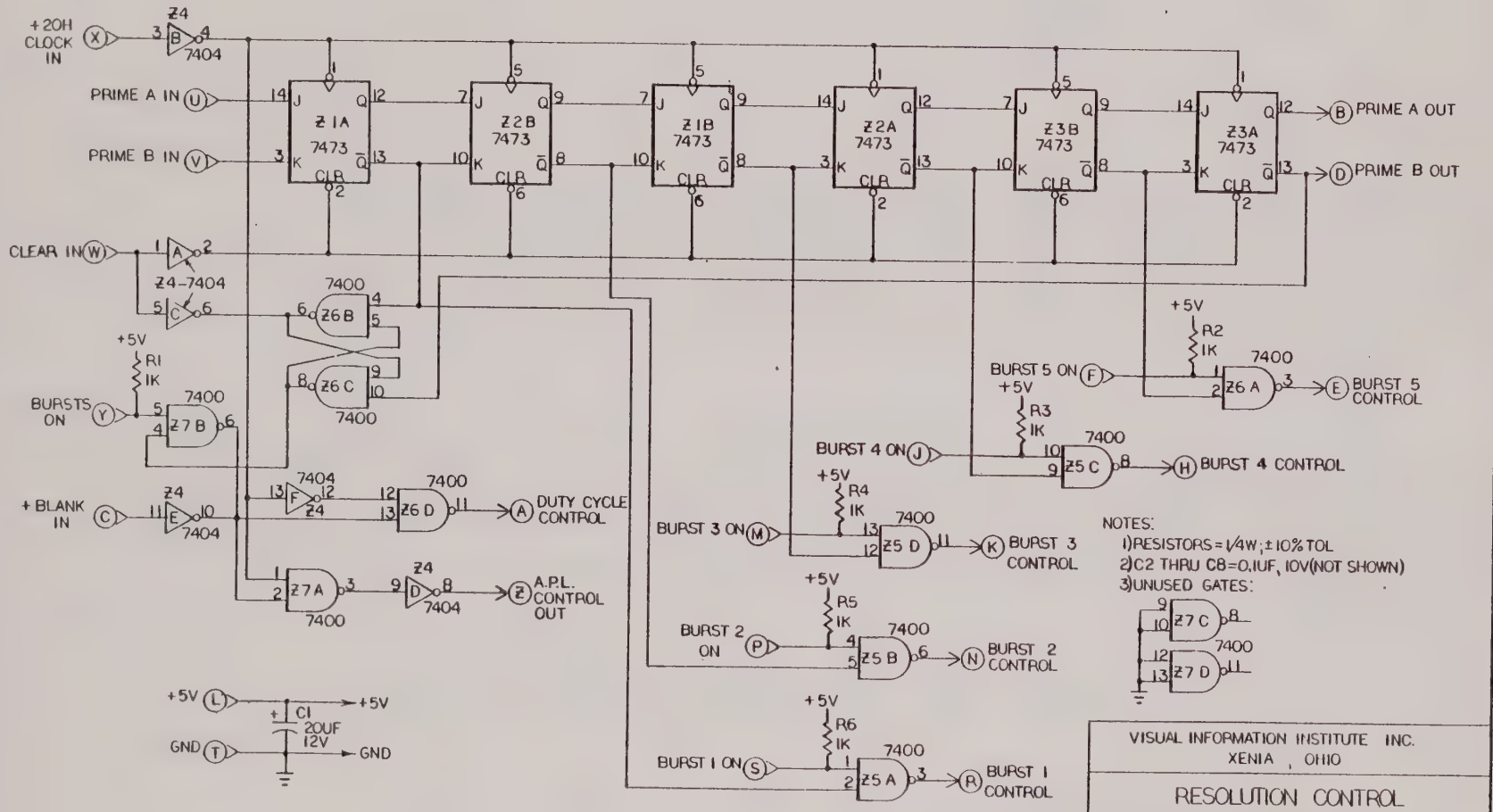
NOTES:

1) RESISTORS = 1/4W ; ±10% TOL.
2) C2 THRU C8 = 0.1UF, 10V
3) o—o = BUS WIRE JUMPER, #22 AWG SOLID
4) SOLDER ON BOTH SIDES OF BOARD
   ▲ = COMP. FEED THRU.
   ■ = #22 AWG WIRE, FEED THRU.

POSITION 7B 4002 RESOLUTION CONTROL (Group 0)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	BURST CONTROL . .	(GRAY SCALE, PIN D)
Y	BURSTS ON	(CONTROL PANEL, S2, RESOLUTION REP RATE 5)
X	+20H CLOCK IN . .	(VIDEO CLOCK, PIN N)
W	CLEAR IN	(VIDEO CLOCK, PIN E)
V	PRIME B IN	(VIDEO CLOCK, PIN L)
U	PRIME A IN	(VIDEO CLOCK, PIN K)
T	GROUND	(GROUND BUSS)
S	BURST 1 ON	(CONTROL PANEL, S2, RESOLUTION REP RATE 1)
R	BURST 1 CONTROL .	(RESOLUTION (7C), PIN Z)
P	BURST 2 ON	(CONTROL PANEL, S2, RESOLUTION REP RATE 2)
N	BURST 2 CONTROL .	(RESOLUTION (7C), PIN Y)
M	BURST 3 ON	(CONTROL PANEL, S2, RESOLUTION REP RATE 3)
L	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
K	BURST 3 CONTROL .	(RESOLUTION (7C), PIN X)
J	BURST 4 ON	(CONTROL PNAEL, S2, RESOLUTION REP RATE 4)
H	BURST 4 CONTROL .	(RESOLUTION (7C), PIN W)
F	BURST 5 ON	(CONTROL PANEL, S2, RESOLUTION REP RATE 5)
E	BURST 5 CONTROL .	(RESOLUTION (7C), PIN V)
D	PRIME B OUT . . .	(VIDEO CLOCK, PIN Y)
C	+BLANK	(CLOCKED BAR/DOT, PIN J)(RESOLUTION (7C), PIN R)(CHARACTER, PIN Z) (PULSE OUTPUT, PIN D)(TTL PULSE OUTPUT, PIN D)(uP INTERFACE (P1), PIN 6)
B	PRIME A OUT . . .	(VIDEO CLOCK, PIN X)
A	DUTY CYCLE	(RESOLUTION (7C), PIN P)



VISUAL INFORMATION INSTITUTE INC. XENIA, OHIO	
RESOLUTION CONTROL	
DRN. D.W.	DATE 9-21 84
APPV'D	DATE 10-1-84
P.C. ART REV. A(8-84)	DWG NO. S-4002
REV.	

CLOCKED BAR/DOT
PRINTED CIRCUIT BOARD ASSEMBLY

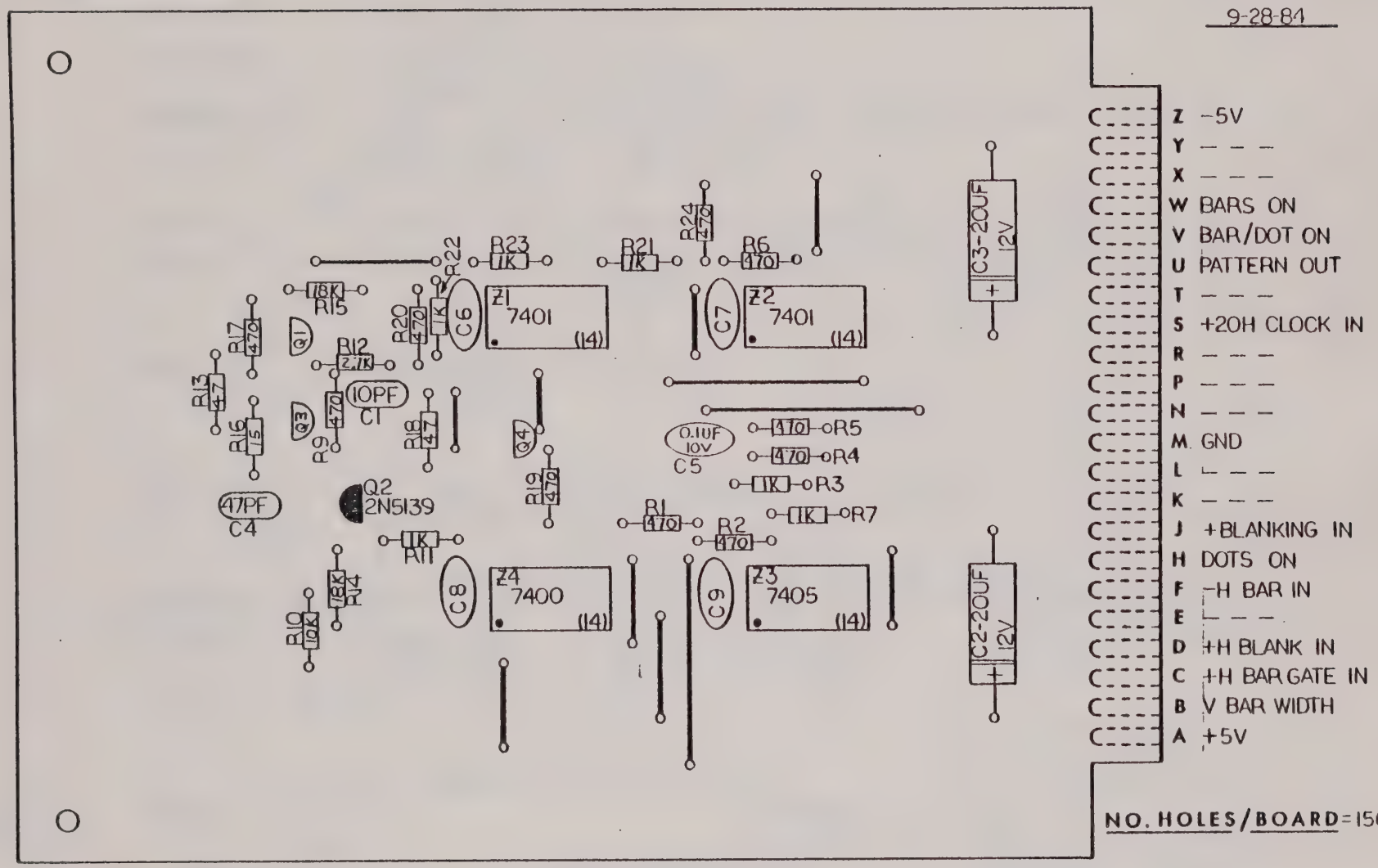
PARTS LIST PL-4003

ARTWORK REV. A (8/84) 9/28/84 SHT 1 OF 1

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	2	3	4	MFR.	Vii DWG.NO.
PCB ASSEMBLY		x	x	x	x	Vii	L-4003
PCB ARTWORK	COND. SIDE	x	x	x	x	Vii	CB-4003
PCB ARTWORK	COMP. SIDE	x	x	x	x	Vii	CF-NONE
PCB SCHEMATIC		x	x	x	x	Vii	S-4003
Transistor	2N5134	3	3	3	3	BAS	A-1844
"	2N5139	1	1	1	1	BAS	A-1845
Resistor, Fixed	15 ohms	1	1	1	1	BAS	A-1450
"	47 ohms	2	2	2	2	BAS	A-1450
"	470 ohms	10	10	10	10	BAS	A-1450
"	1K ohms	6	6	6	6	BAS	A-1450
"	2.7K ohms	1	1	1	1	BAS	A-1450
"	10K ohms	1	1	1	1	BAS	A-1450
"	18K ohms	2	2	2	2	BAS	A-1450
Resistor, Var.	5K ohms	1	x	1	x	BAS	A-1460
Capacitor	0.1uf, 10v	5	5	4	4	BAS	A-1455
"	20uf, 12v	2	2	2	2	BAS	A-1458
"	10 pf	1	1	1	1	BAS	A-1454
"	47 pf	1	1	1	1	BAS	A-1454
I.C. Socket	14 pin	4	4	3	3	BAS	A-1465
I.C.	7400	1	1	x	x	BAS	A-1747
"	7401	2	2	2	2	BAS	
"	7405	1	1	1	1	BAS	A-1757
Bus Wire, Jumper	#22 Awg Solid	12	12	12	12	BAS	

CLOCKED BAR/DOT REV. A(8-84) DWG. NO. L-4003 (GROUP 2)

PARTS LIST
9-28-84



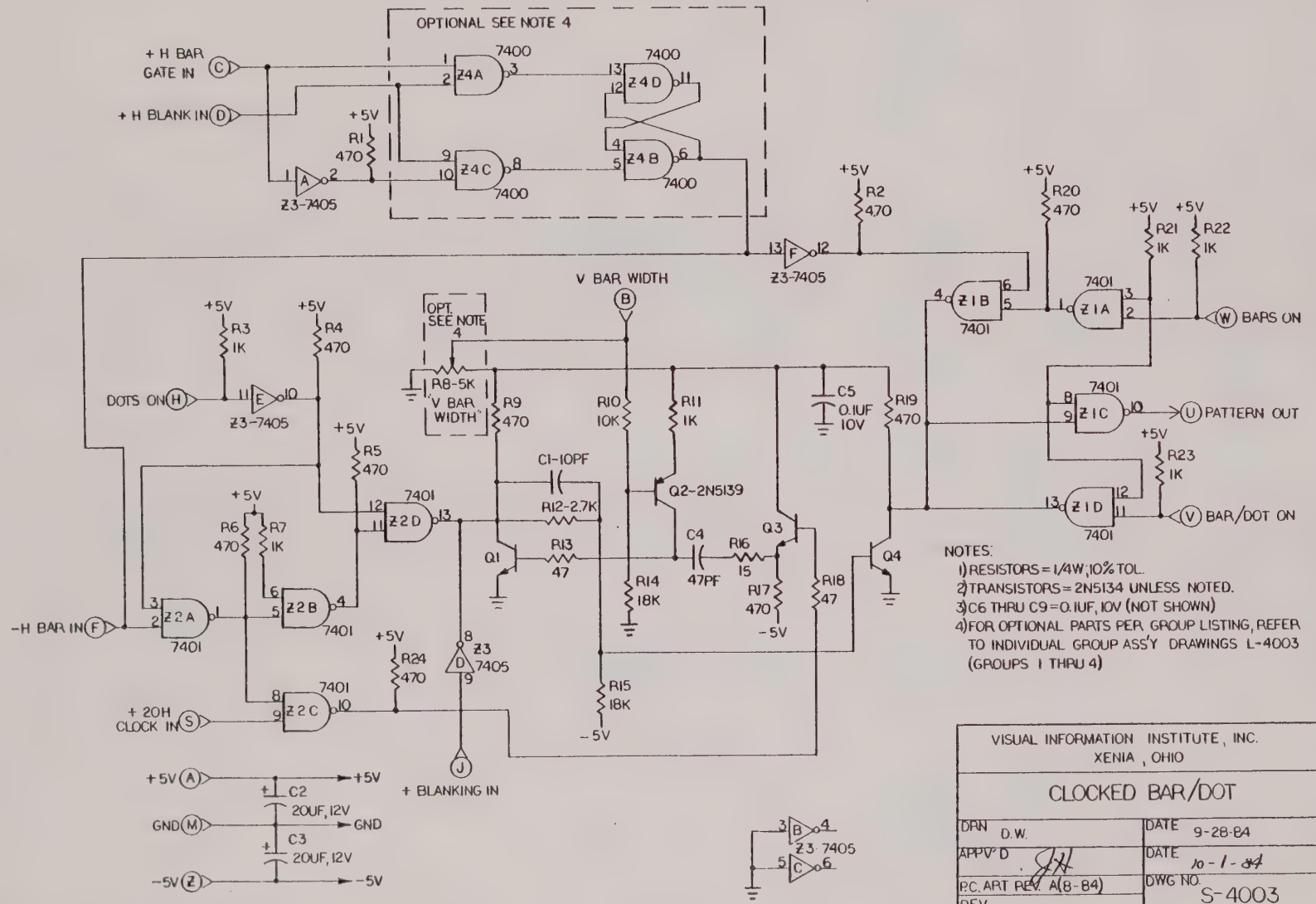
NO. HOLES/BOARD=156

NOTES:
1) TRANSISTORS = 2N5134 UNLESS NOTED OTHERWISE.
2) RESISTORS = 1/4 W; ± 10% TOL.
3) C6 THRU C9 = 0.1UF, 10V
4) o—o = JUMPER, #22AWG WIRE SOLID

POSITION 8B 4003 CLOCKED BAR/DOT (Group 2)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
Y	--	
X	--	
W	BARS ON	(CONTROL PANEL, S3, FUNCTION SELECT - BARS)
V	BAR/DOT ON	(CONTROL PANEL, S3, FUNCTION SELECT)
U	PATTERN OUT . . .	(VIDEO CLOCK, PIN R)(GRAY SCALE, PIN L)(PATTERN LOGIC, PIN Z) (TTL VIDEO (3C,4C,5C), PIN P)(CLOCKED COLOR BAR, PIN B)
T	--	
S	20H CLOCK IN . .	(CLOCKED BAR/DOT, PIN E)(uP INTERFACE (P1), PIN P)
R	--	
P	--	
N	--	
M	GROUND	(GROUND BUSS)
L	--	
K	--	
J	+BLANK	(RESOLUTION CONTROL, PIN C)(RESOLUTION (7C,9C), PIN R)(CHARACTER, PIN Z)
H	DOTS ON	(CONTROL PANEL, S3, FUNCTION SELECT - DOTS)
F	--	
E	20H CLOCK IN . . .	(CLOCKED BAR/DOT, PIN S)(uP INTERFACE (P1), PIN P)
D	+H BLANK IN . . .	(VIDEO CLOCK, PIN F)(GRAY SCALE SELECT, PIN D)(CLOCKED COLOR BAR, PIN J) (CHARACTER, PIN X)(uP INTERFACE (P1), PIN 4)
C	+H BAR GATE IN . .	(uP INTERFACE (P1), PIN 10)
B	V BAR WIDTH . . .	(CONTROL PANEL, R1, DOT WIDTH)
A	+5v.	(+5v. BUSS)(POWER REGULATOR PIN A)(CONTROL PANEL, R1, DOT WIDTH)
	GROUND	(uP INTERFACE (P1), PINS Y, 21)


OPTIONAL SEE NOTE 4
+ H BAR GATE IN
+ H BLANK IN
+5V
R1 470
Z3-7405
7400
Z4A
Z4C
Z4D
Z4B
+5V
R2 470
Z3-7405
V BAR WIDTH
OPT. SEE NOTE 4
R8-5K "V BAR WIDTH"
+5V
R3 1K
R4 470
DOTS ON
Z3-7405
+5V
R5 470
+5V
R6 470
R7 1K
7401
Z2A
Z2B
Z2C
Z2D
-H BAR IN
+ 20H CLOCK IN
+5V
R24 470
Z3 7405
+ BLANKING IN
R9 470
R10 10K
R11 1K
C1-10PF
R12-2.7K
Q2-2N5139
Q1
R13 47
C4 47PF
R16 15
Q3
R17 470
-5V
R14 18K
R15 18K
-5V
C5 0.1UF 10V
R19 470
Q4
R18 47
+5V
R20 470
+5V
R21 1K
+5V
R22 1K
Z1A
Z1B
Z1C
Z1D
W BARS ON
U PATTERN OUT
+5V
R23 1K
V BAR/DOT ON
NOTES:
1) RESISTORS = 1/4W, 10% TOL.
2) TRANSISTORS = 2N5134 UNLESS NOTED.
3) C6 THRU C9 = 0.1UF, 10V (NOT SHOWN)
4) FOR OPTIONAL PARTS PER GROUP LISTING, REFER TO INDIVIDUAL GROUP ASS'Y DRAWINGS L-4003 (GROUPS 1 THRU 4)
+5V
GND
-5V
C2 20UF, 12V
C3 20UF, 12V
Z3 7405
VISUAL INFORMATION INSTITUTE, INC.
XENIA, OHIO
CLOCKED BAR/DOT
DRN D.W.
DATE 9-28-84
APPV'D
DATE 10-1-84
P.C. ART REV. A(8-84)
DWG NO. S-4003
REV.

PATTERN LOGIC
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-4006

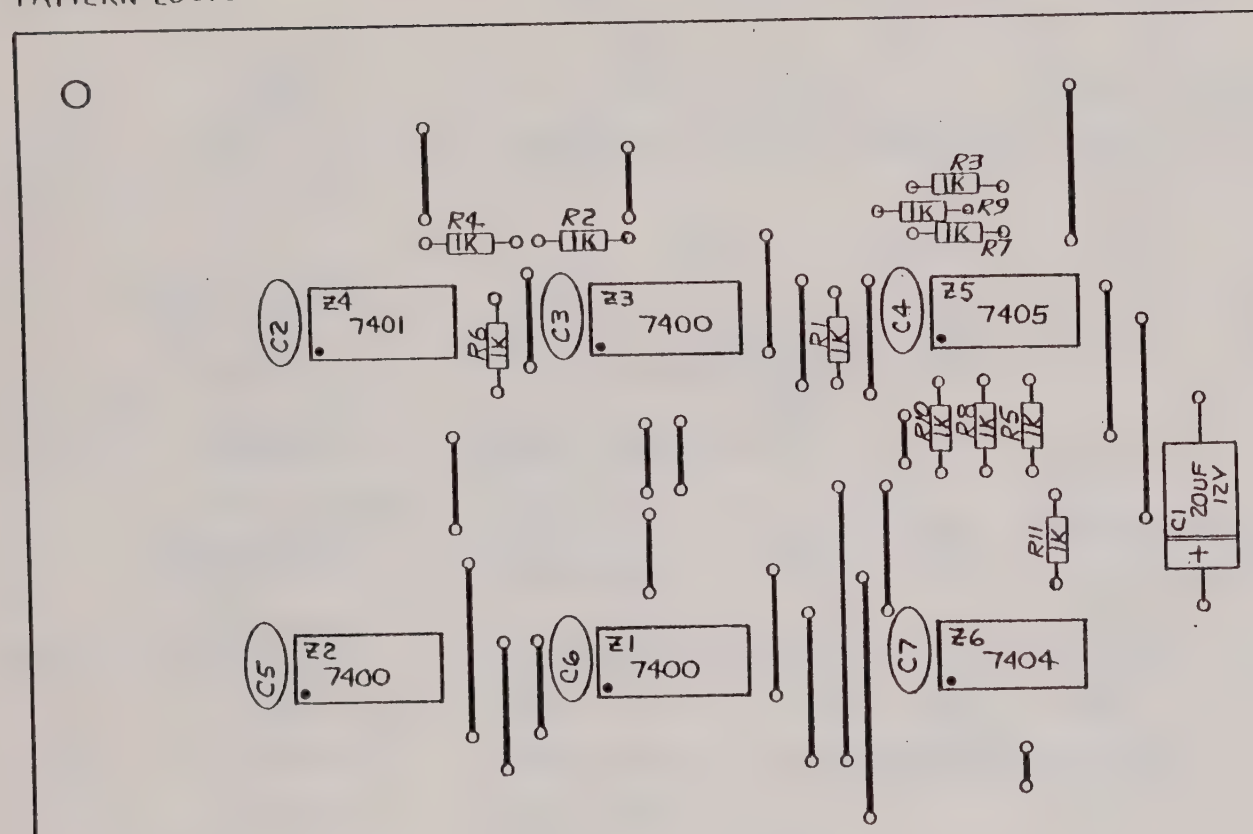
ARTWORK REV. A (7/84) 8/20/84 SHT 1 OF 1

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	QTY/GROUP 2	MFR.	Vii DWG. NO.
PCB ASSEMBLY		x	x	Vii	L-4006
PCB ARTWORK	CONDUCT SIDE	x	x	Vii	CB-4006
PCB ARTWORK	COMP. SIDE	x	x	Vii	CF-NONE
PCB SCHEMATIC		x	x	Vii	S-4006
Resistor	1K ohms	11	11	BAS	A-1450
Capacitor	20uf, 12v	1	1	BAS	A-1458
Capacitor	0.1uf, 10v	6	4	BAS	A-1455
I.C. Socket	14 pin	6	4	BAS	A-1465
I.C.	7400	3	1	BAS	A-1747
I.C.	7401	1	1	BAS	
I.C.	7404	1	1	BAS	
I.C.	7405	1	1	BAS	A-1754
Bus Wire, Jumper	#22 Awg Solid	23	17	BAS	

PATTERN LOGIC

REV. A (7-84) DWG. NO. L-4006 (GROUP I)

PARTS LIST
8-20-84



Z	WINDOW OUTPUT
Y	WINDOW ON
X	+H WINDOW GATE IN
W	V STRIPE ON
V	VIDEO ON
U	COLOR BAR ON
T	V WINDOW ON
S	GND
R	COMB. ON
P	COLOR BAR CONTROL OUT
N	VIDEO CONTROL OUT
M	— — —
L	+5V
K	— — —
J	— — —
H	+V WINDOW IN/OUT
F	+A.P.L. IN/OUT
E	-BLANK IN
D	+V WINDOW GATE IN
C	+A.P.L. GATE IN
B	— — —
A	— — —

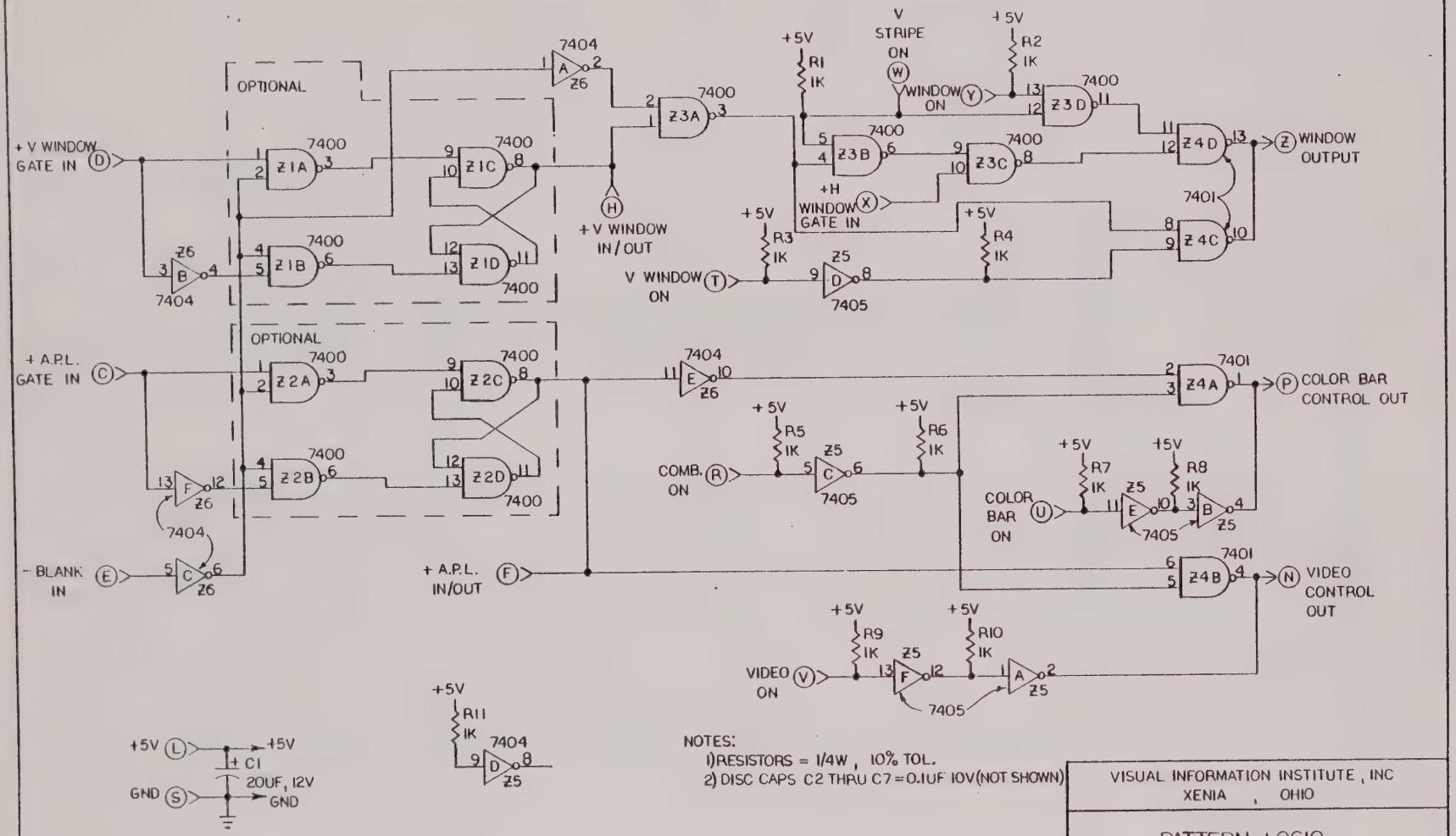
NO. HOLES/BOARD=166

NOTES:
1) RESISTORS = 1/4W ; 10% TOL.
2) DISC CAPS = 0.1UF, 10V
3) o—o = BUS WIRE JUMPER, #22 AWG, SOLID.

POSITION 9B 4006 PATTERN LOGIC (Group 1)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	WINDOW OUT	(CLOCKED BAR/DOT, PIN U)(VIDEO CLOCK, PIN R)(GRAY SCALE, PIN L) (TTL VIDEO (3C,4C,5C), PIN P)(CLOCKED COLOR BAR, PIN B)
Y	WINDOW ON	(PATTERN LOGIC, PIN T)
X	+H WINDOW IN . . .	(uP INTERFACE (P1), PIN 5)
W	V STRIPE ON	(CONTROL PANEL, S3, FUNCTION SELECT - V STRIPE)
V	VIDEO ON	(CONTROL PANEL, S3, FUNCTION SELECT - VIDEO)
U	COLOR BAR ON . . .	(CONTROL PANEL, S3, FUNCTION SELECT - COLOR BARS)
T	V WINDOW ON	(CONTROL PANEL, S3, FUNCTION SELECT - WINDOW)
S	GROUND	(GROUND BUSS)
R	COMBINATION ON . .	(CONTROL PANEL, S3, FUNCTION SELECT - COMBINATION)
P	COLOR BAR CONTROL .	(CLOCKED COLOR BAR, PIN F)
N	VIDEO CONTROL . . .	(VIDEO CLOCK, PIN P).
M	--	
L	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
K	--	
J	--	
H	--	
F	--	
E	-BLANK IN	(VIDEO CLOCK, PIN B)(uP INTERFACE (P1), PIN F)
D	+V WINDOW IN . . .	(uP INTERFACE (P1), PIN E)
C	+APL GATE IN . . .	(uP INTERFACE (P1), PIN 11)
B	--	
A	--	



NOTES:
1) RESISTORS = 1/4W, 10% TOL.
2) DISC CAPS C2 THRU C7 = 0.1UF 10V (NOT SHOWN)

VISUAL INFORMATION INSTITUTE, INC XENIA, OHIO	
PATTERN LOGIC	
DRN D WARNER	DATE 8-20-84
APPV'D JH	DATE 8-26-84
P.C. REV. A (7-84)	DWG NO. S-4006
REV.	

POWER REGULATOR
PRINTED CIRCUIT BOARD ASSEMBLY

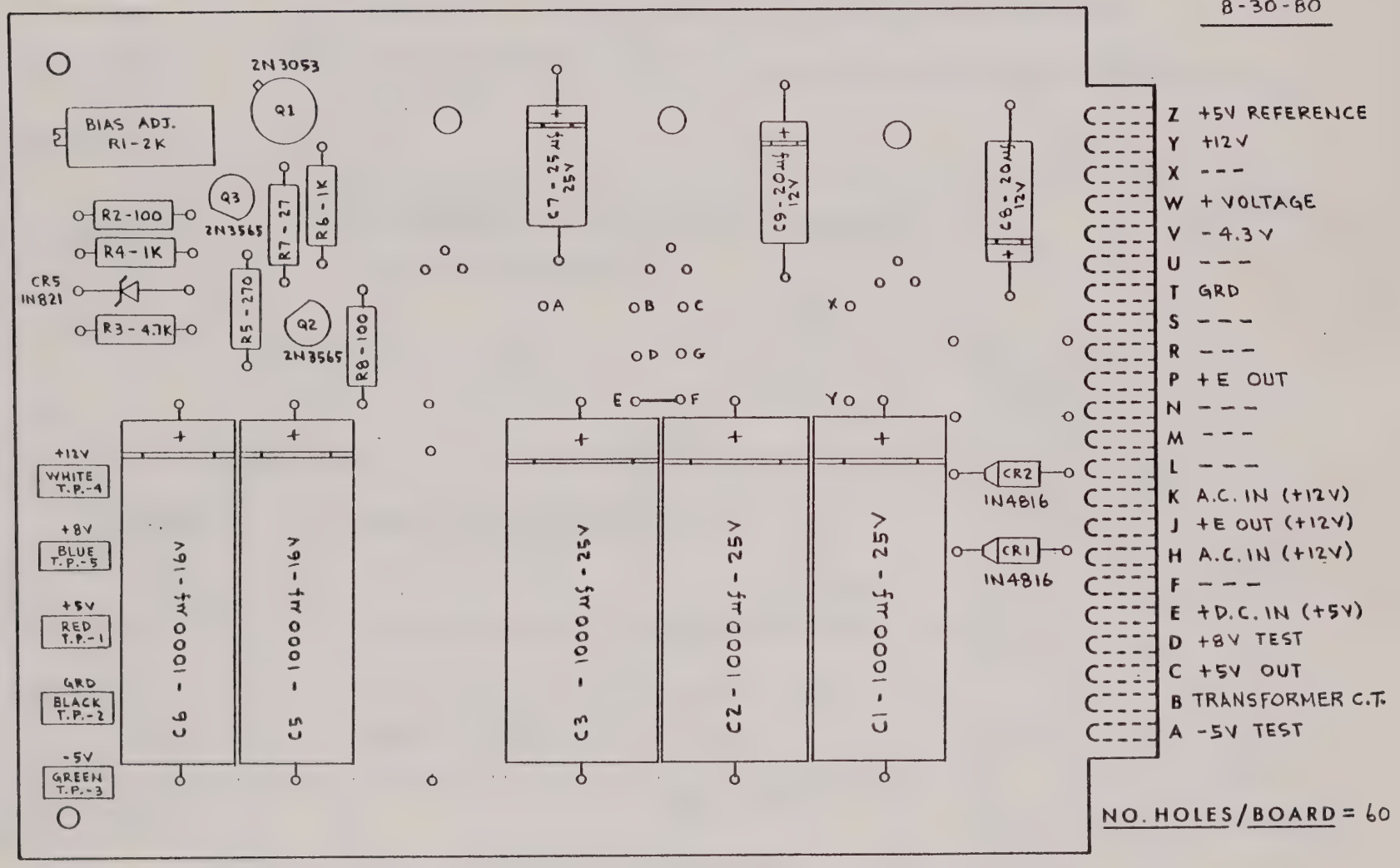
PARTS LIST PL-2110

ARTWORK REV. A (7/80) 8/30/80 SHT 1 of 1

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	2	3	MFR.	Vii DWG.NO.
PCB ASSEMBLY		x	x	x	Vii	L-2110
PCB ARTWORK	COND. SIDE	x	x	x	Vii	CB-2110
PCB ARTWORK	COMP. SIDE	x	x	x	Vii	CF-NONE
PCB SCHEMATIC		x	x	x	Vii	S-2110
Hole Count		60	60	56		
Diode	1N4816	2	4	2	BAS	A-1853
Diode, Zener	1N821	1	1	1	BAS	
Transistor	2N3053	1	1	1	BAS	A-1834
"	2N3565	2	2	2	BAS	A-1776
Resistor, Fixed	27 ohms	1	1	1	BAS	A-1450
"	100 ohms	2	2	2	BAS	A-1450
"	270 ohms	1	1	1	BAS	A-1450
"	1K ohms	2	2	2	BAS	A-1450
"	4.7K ohms	1	1	1	BAS	A-1450
Resistor, Var.	2K ohms	1	1	1	BAS	A-1460
Capacitor	20uf, 12v	2	1	1	BAS	A-1458
"	25uf, 25v	1	1	1	BAS	A-1458
"	500uf, 25v	x	1	x	BAS	A-1459
	1000uf, 16v	2	2	2	BAS	A-1459
"	1000uf, 25v	3	3	3	BAS	A-1459
Test Points	Red	1	1	1	BAS	A-1766
"	Black	1	1	1	BAS	A-1766
"	Green	1	1	1	BAS	A-1766
"	White	1	1	1	BAS	A-1766
"	Blue	1	x	x	BAS	A-1766
Bus wire, jumper	#24 Awg Sld	1	x	1	BAS	

POWER REGULATOR 7-80 REV. A DWG. NO. L-2110 (GROUP 1)

PARTS LIST
8-30-80



NO. HOLES/BOARD = 60

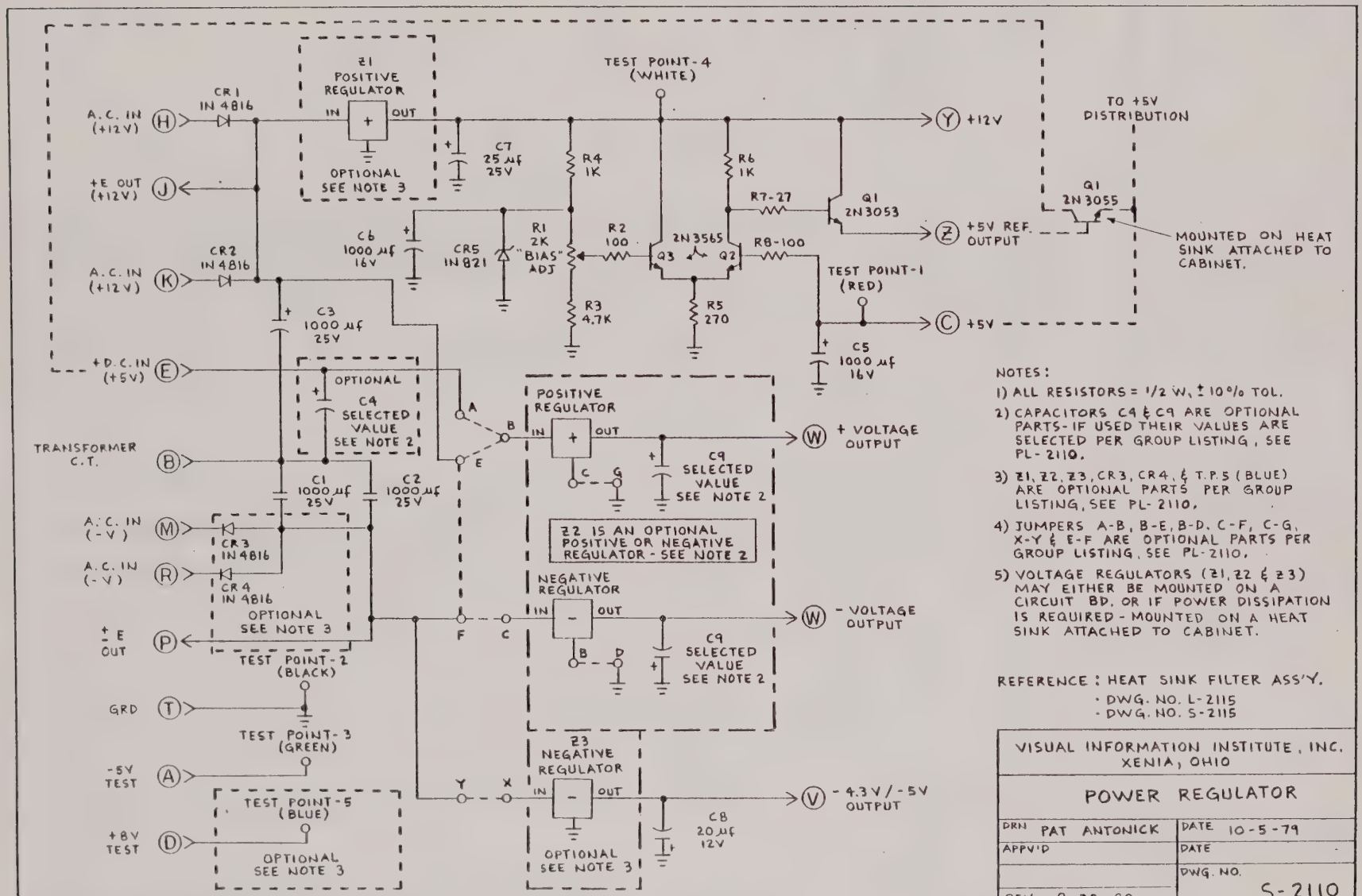
NOTES: 1) ALL RESISTORS = ½ W, ± 10% TOL.

2) o—o BUS WIRE, #24 SOLID.

POSITION 2C 2110 POWER REGULATOR (Group 1)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	+5v. REF	(HEAT SINK, RIGHT SIDE, +5v. REF)
Y	+12v.	(+12v. BUSS)(HEAT SINK, LEFT SIDE, +12v.)
X	--	
W	+8v.	(TTL VIDEO (3C,4C,5C), PIN L)(POWER REGULATOR, PIN D)
V	--	
U	--	
T	GROUND	(GROUND BUSS)
S	--	
R	--	
P	--	
N	--	
M	--	
L	--	
K	A.C.2	(CHASSIS, TB1, POSITION 7)
J	+D.C.	(PULSE OUTPUT, PIN Y)(HEAT SINK, LEFT SIDE, +E)
H	A.C.2	(CHASSIS, TB1, POSITION 5)
F	--	
E	--	
D	+8v.	(POWER REGULATOR, PIN W)(TTL VIDEO (3C,4C,5C), PIN L)(HEAT SINK, RIGHT SIDE, +8v.)
C	+5v.	(+5v. BUSS)(HEAT SINK, RIGHT SIDE, +5v.)
B	C.T.	(CHASSIS, TB1, POSITION 6)(HEAT SINK, CENTER, GROUND)(GROUND BUSS)
A	-5v.	(-5v. BUSS)(HEAT SINK, LEFT SIDE, -5v.)
	GROUND	(HEAT SINK, LEFT SIDE, GROUND)(REAR PANEL, J4, GROUND)(CONTROL PANEL, R1, DOT WIDTH)



NOTES:

1) ALL RESISTORS = 1/2 W, ± 10% TOL.
2) CAPACITORS C4 & C9 ARE OPTIONAL PARTS - IF USED THEIR VALUES ARE SELECTED PER GROUP LISTING, SEE PL-2110.
3) Z1, Z2, Z3, CR3, CR4, & T.P.5 (BLUE) ARE OPTIONAL PARTS PER GROUP LISTING, SEE PL-2110.
4) JUMPERS A-B, B-E, B-D, C-F, C-G, X-Y & E-F ARE OPTIONAL PARTS PER GROUP LISTING, SEE PL-2110.
5) VOLTAGE REGULATORS (Z1, Z2 & Z3) MAY EITHER BE MOUNTED ON A CIRCUIT BD. OR IF POWER DISSIPATION IS REQUIRED - MOUNTED ON A HEAT SINK ATTACHED TO CABINET.

REFERENCE: HEAT SINK FILTER ASS'Y.
- DWG. NO. L-2115
- DWG. NO. S-2115

VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
POWER REGULATOR	
DRN PAT ANTONICK	DATE 10-5-79
APPV'D	DATE
	DWG. NO. S-2110
REV. 8-30-80	

TTL VIDEO
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-2155

ARTWORK REV. A (7/83) 4/1/85 SHT 1 OF 2

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	2	3	4	5	6	7	8	9	10	MFR	Vii DWG.NO.
PCB ASSEMBLY		x	x	x	x	x	x	x	x	x	x	Vii	L-2155
PCB ARTWORK	COND. SIDE	x	x	x	x	x	x	x	x	x	x	Vii	CB-2155
PCB ARTWORK	COMP. SIDE	x	x	x	x	x	x	x	x	x	x	Vii	CF-NONE
PCB SCHEMATIC		x	x	x	x	x	x	x	x	x	x	Vii	S-2155
HOLE COUNT		246	245	248	247	233	227	259	260	256	257		
Diode	1N4154	8	8	8	8	8	8	8	8	8	8	BAS	A-1797
Transistor, NPN	2N3646	1	1	1	1	1	1	1	1	1	1	BAS	A-1797
" , NPN	2N3866	1	1	1	1	1	1	2	2	2	2	BAS	A-1859
" , NPN	2N5134	11	11	11	11	9	9	10	10	10	10	BAS	A-1844
" , PNP	2N5139	5	5	5	5	5	5	5	5	5	5	BAS	A-1845
" , PNP	2N5771	2	2	2	2	2	2	2	2	2	2	BAS	A-1850
Resistor, Fixed	10 ohms	2	2	2	2	2	2	2	2	2	2	BAS	A-1450
"	27 ohms	3	3	3	3	3	3	3	3	3	3	BAS	A-1450
"	47 ohms	2	2	2	2	2	2	2	2	2	2	BAS	A-1450
"	68 ohms	1	1	1	1	1	1	1	1	1	1	BAS	A-1450
"	100 ohms	13	13	13	13	13	13	16	16	16	16	BAS	A-1450
"	150 ohms	4	4	4	4	4	4	3	3	3	3	BAS	A-1450
"	220 ohms	2	2	2	2	2	2	5	5	4	4	BAS	A-1450
"	270 ohms	6	6	6	6	6	6	5	5	5	5	BAS	A-1450
"	330 ohms	1	1	1	1	1	1	x	x	x	x	BAS	A-1450
"	390 ohms	1	1	1	1	1	1	1	1	1	1	BAS	A-1450
"	470 ohms	8	7	8	7	6	6	3	4	3	4	BAS	A-1450
"	680 ohms	1	1	1	1	1	1	1	1	1	1	BAS	A-1450
"	1K ohms	3	3	3	3	3	3	4	4	4	4	BAS	A-1450
"	1.5K ohms	1	1	1	1	1	x	3	3	3	3	BAS	A-1450
"	2.7K ohms	4	4	4	4	2	2	2	2	2	2	BAS	A-1450
"	3.3K ohms	1	1	1	1	1	1	1	1	1	1	BAS	A-1450
"	6.8K ohms	1	1	1	1	1	1	1	1	1	1	BAS	A-1450
"	10K ohms	1	1	1	1	x	x	1	1	1	1	BAS	A-1450
"	12K ohms	x	x	x	x	x	x	2	2	2	2	BAS	A-1450
"	18K ohms	4	4	4	4	3	3	2	2	2	2	BAS	A-1450
Resistor, Fixed	330, 1/2w	x	x	x	x	x	x	1	1	1	1	BAS	A-1451
Resistor, Var.	1K ohms	x	x	2	2	2	2	2	2	1	1	BAS	A-1460
"	2K ohms	x	1	x	1	1	x	1	x	1	x	BAS	A-1460
"	5K ohms	2	2	2	2	2	1	2	2	2	2	BAS	A-1460

TTL VIDEO
PRINTED CIRCUIT BOARD ASSEMBLY

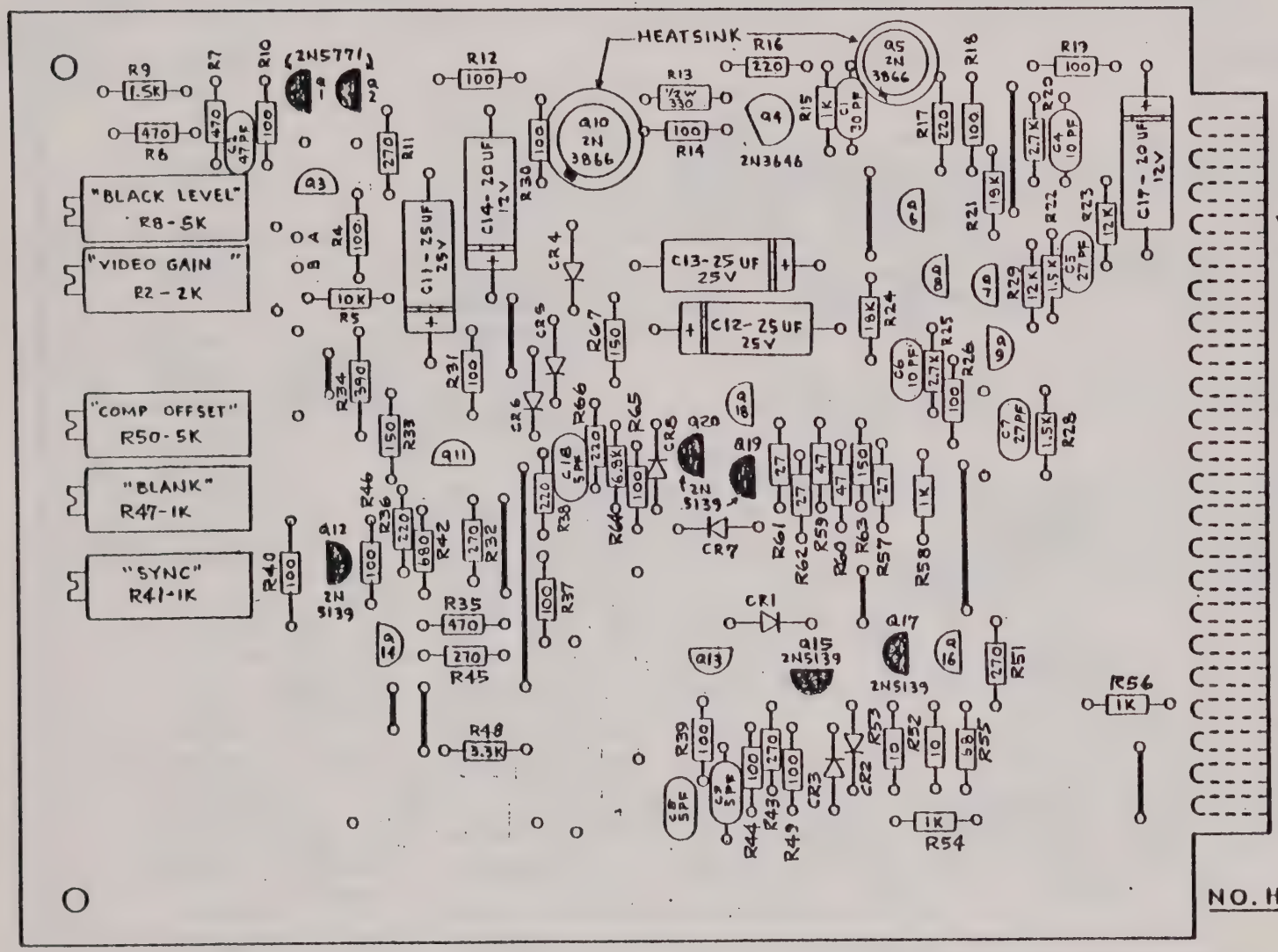
PARTS LIST PL-2155

ARTWORK REV. A (7/83) 4/1/85 SHT 2 OF 2

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	2	3	4	5	6	7	8	9	10	MFR	Vii-DWG.NO.
Capacitor	5 pf	3	3	3	3	3	3	3	3	3	3	BAS	A-1454
"	10 pf	x	x	x	x	x	x	2	2	2	2	BAS	A-1454
"	27 pf	x	x	x	x	x	x	2	2	2	2	BAS	A-1454
"	30 pf	x	x	x	x	x	x	1	1	1	1	BAS	A-1454
"	47 pf	1	1	1	1	1	1	1	1	1	1	BAS	A-1454
"	20uf, 12v	2	2	2	2	2	2	2	2	2	2	BAS	A-1458
"	25uf, 25v	3	3	3	3	3	3	3	3	3	3	BAS	A-1458
Bus wire, jumper	#22 Awg Sld	14	13	12	11	12	13	11	12	12	13	BAS	

TTL VIDEO 7-83 REV. A DWG. NO. L-2155 (GROUP 7)

PARTS LIST
4-1-85

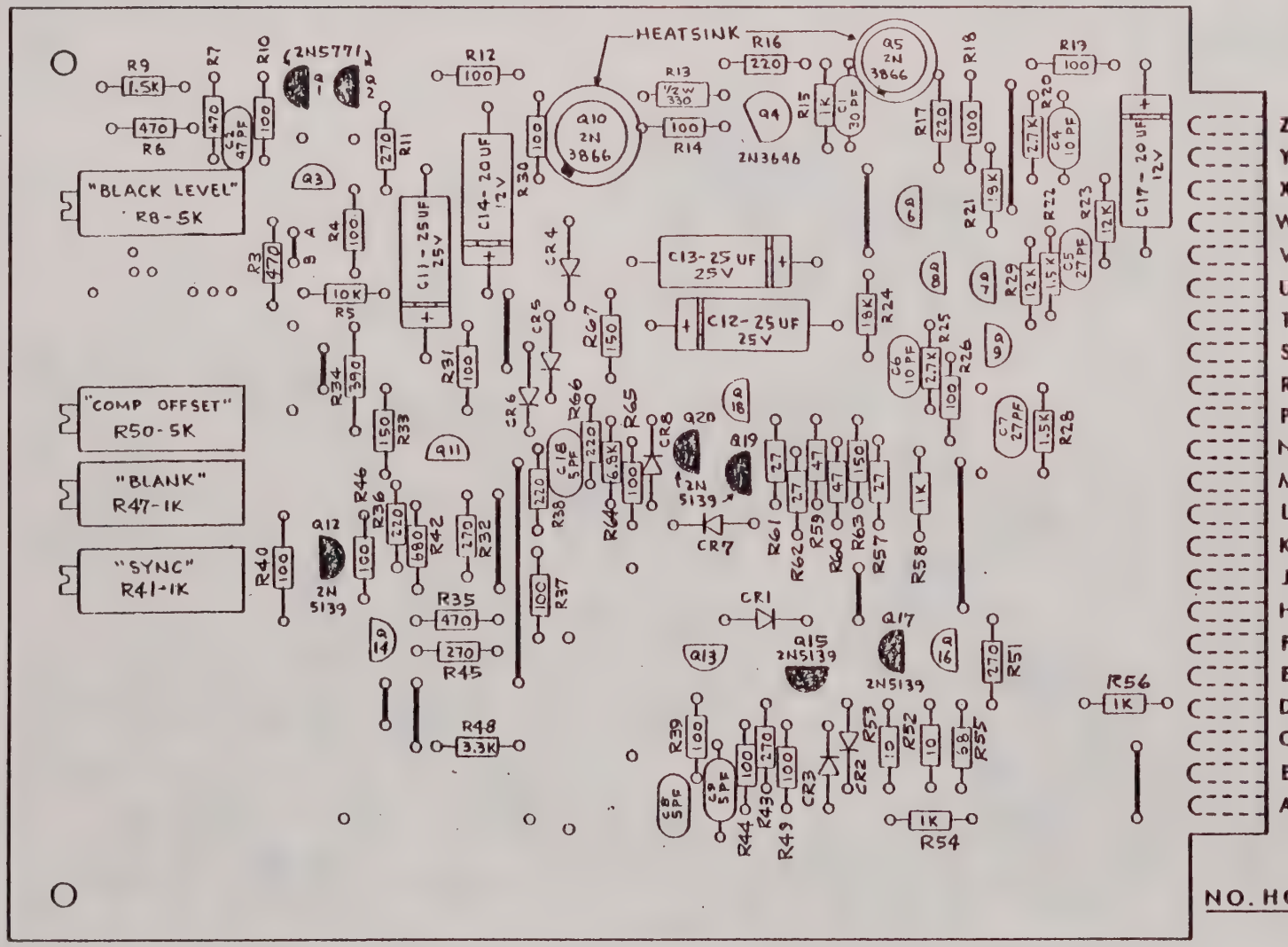


NO. HOLES/BOARD = 259

NOTES: 1) ALL DIODES = IN4154.
2) ALL TRANSISTORS = 2N5134, UNLESS NOTED.
3) ALL RESISTORS = 1/4W, ±10% TOL.
4) o—o BUS WIRE, #24 AWG, SOLID.
5) RESISTOR R38 NOT NORMALLY USED. SELECT VALUE DESIRED TO ATTENUATE OVERALL SIGNAL LEVEL.

TTL VIDEO 7-83 REV. A DWG. NO. L-2155 (GROUP 8)

PARTS LIST
4-1-85



NO. HOLES/BOARD=260

NOTES: 1) ALL DIODES = IN4154.
2) ALL TRANSISTORS = 2N5134, UNLESS NOTED.
3) ALL RESISTORS = 1/4W, ±10% TOL.
4) o—o BUS WIRE, #24 AWG. SOLID.
5) RESISTOR R38 NOT NORMALLY USED. SELECT VALUE DESIRED TO ATTENUATE OVERALL SIGNAL LEVEL.

POSITION 3C 2155 TTL VIDEO R (Group 7)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
Y	R IN	(CLOCKED COLOR BAR, PIN L)
X	GROUND	(TTL VIDEO (3C), PINS V, N, F, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
W	RESOLUTION IN . .	(CLOCKED COLOR BAR, PIN T)
V	GROUND	(TTL VIDEO (3C), PINS X, N, F, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)
U	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
T	--	
S	+BLANK IN	(TTL VIDEO (4C,5C), PIN S)(VIDEO CONTROL, PINS N, C)(VIDEO CLOCK, PIN C)
R	--	
P	PATTERN IN . . .	(TTL VIDEO (4C,5C), PIN P)(CLOCKED COLOR BAR, PIN B)(GRAY SCALE, PIN L) (VIDEO CLOCK, PIN R)(CLOCKED BAR/DOT, PIN U)(PATTERN LOGIC, PIN Z)
N	GROUND	(TTL VIDEO (3C), PINS X, V, F, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
M	TTL OUT - R . .	(REAR PANEL, J8, TTL VIDEO R)
L	+8v. IN	(POWER REGULATOR, PINS W, D)(TTL VIDEO (4C,5C), PIN L)
K	GRAY SCALE IN . .	(TTL VIDEO (4C,5C), PIN K)(VIDEO CONTROL, PIN Z)
J	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
H	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
F	GROUND	(TTL VIDEO (3C), PINS X, V, N, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
E	VIDEO OUT	(REAR PANEL, J6, COMPOSITE VIDEO R)
D	VIDEO R	(CONTROL PANEL, TP5, VIDEO R)
C	BLANK IN	(TTL VIDEO (4C,5C), PIN C)(VIDEO CONTROL, PIN L)
B	GROUND	(TTL VIDEO (3C), PINS X, V, N, F)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
A	SYNC IN	(TTL VIDEO (4C,5C), PIN A)(VIDEO CONTROL, PIN F)

POSITION 4C 2155 TTL VIDEO G (Group 8)

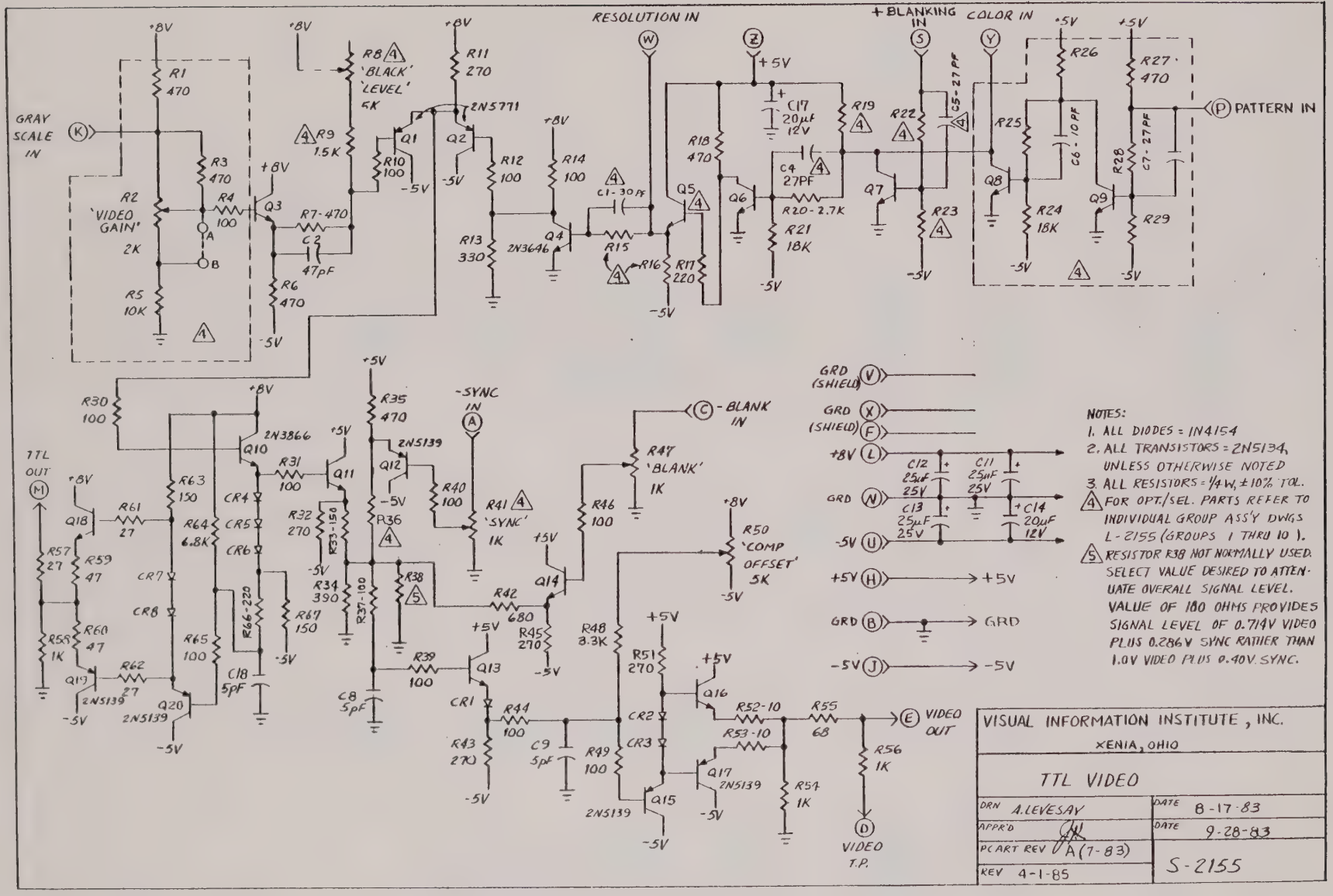
MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
Y	G IN	(CLOCKED COLOR BAR, PIN N)
X	GROUND	(TTL VIDEO (4C), PINS V, N, F, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
W	RESOLUTION IN . . .	(CLOCKED COLOR BAR, PIN V)
V	GROUND	(TTL VIDEO (4C), PINS X, N, F, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
U	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
T	--	
S	+BLANK IN	(TTL VIDEO (3C,5C), PIN S)(VIDEO CONTROL, PINS N, C)(VIDEO CLOCK, PIN C)
R	--	
P	PATTERN IN	(TTL VIDEO (3C,5C), PIN P)(CLOCKED COLOR BAR, PIN B)(GRAY SCALE, PIN L) (VIDEO CLOCK, PIN R)(CLOCKED BAR/DOT, PIN U)(PATTERN LOGIC, PIN Z)
N	GROUND	(TTL VIDEO (4C), PINS X, V, F, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
M	TTL OUT - R	(REAR PANEL, J9, TTL VIDEO G)
L	+8v. IN	(POWER REGULATOR, PINS W, D)(TTL VIDEO (3C,5C), PIN L)
K	GRAY SCALE IN . . .	(TTL VIDEO (3C,5C), PIN K)(VIDEO CONTROL, PIN Z)
J	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
H	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
F	GROUND	(TTL VIDEO (4C), PINS X, V, N, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
E	VIDEO OUT	(REAR PANEL, J5, COMPOSITE VIDEO G)
D	VIDEO R	(CONTROL PANEL, TP6, VIDEO G)
C	BLANK IN	(TTL VIDEO (3C,5C), PIN C)(VIDEO CONTROL, PIN L)
B	GROUND	(TTL VIDEO (4C), PINS X, V, N, F)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
A	SYNC IN	(TTL VIDEO (3C,5C), PIN A)(VIDEO CONTROL, PIN F)

POSITION 5C 2155 TTL VIDEO B (Group 7)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
Y	B IN	(CLOCKED COLOR BAR, PIN M)
X	GROUND	(TTL VIDEO (5C), PINS V, N, F, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
W	RESOLUTION IN . .	(CLOCKED COLOR BAR, PIN X)
V	GROUND	(TTL VIDEO (5C), PINS X, N, F, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
U	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
T	--	
S	+BLANK IN	(TTL VIDEO (3C,4C), PIN S)(VIDEO CONTROL, PINS N, C)(VIDEO CLOCK, PIN C)
R	--	
P	PATTERN IN . . .	(TTL VIDEO (3C,4C), PIN P)(CLOCKED COLOR BAR, PIN B)(GRAY SCALE, PIN L) (VIDEO CLOCK, PIN R)(CLOCKED BAR/DOT, PIN U)(PATTERN LOGIC, PIN Z)
N	GROUND	(TTL VIDEO (5C), PINS X, V, F, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
M	TTL OUT - R . .	(REAR PANEL, J10, TTL VIDEO B)
L	+8v. IN	(POWER REGULATOR, PINS W, D)(TTL VIDEO (3C,4C), PIN L)
K	GRAY SCALE IN . .	(TTL VIDEO (3C,4C), PIN K)(VIDEO CONTROL, PIN Z)
J	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
H	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
F	GROUND	(TTL VIDEO (5C), PINS X, V, N, B)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
E	VIDEO OUT	(REAR PANEL, J7, COMPOSITE VIDEO B)
D	VIDEO R	(CONTROL PANEL, TP7, VIDEO B)
C	BLANK IN	(TTL VIDEO (3C,4C), PIN C)(VIDEO CONTROL, PIN L)
B	GROUND	(TTL VIDEO (5C), PINS X, V, N, F)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
A	SYNC IN	(TTL VIDEO (3C,4C), PIN A)(VIDEO CONTROL, PIN F)



NOTES:

1. ALL DIODES = IN4154
2. ALL TRANSISTORS = 2N5134, UNLESS OTHERWISE NOTED
3. ALL RESISTORS = 1/4 W, ±10% TOL.
4. FOR OPT./SEL. PARTS REFER TO INDIVIDUAL GROUP ASS'Y DWGS L-2155 (GROUPS 1 THRU 10).
5. RESISTOR R38 NOT NORMALLY USED. SELECT VALUE DESIRED TO ATTENUATE OVERALL SIGNAL LEVEL. VALUE OF 180 OHMS PROVIDES SIGNAL LEVEL OF 0.714V VIDEO PLUS 0.286V SYNC RATHER THAN 1.0V VIDEO PLUS 0.40V SYNC.

VISUAL INFORMATION INSTITUTE, INC.
XENIA, OHIO

TTL VIDEO

DRN A.LEVESAY	DATE 8-17-83
APPR'D	DATE 9-28-83
PC ART REV A(7-83)	S-2155
REV 4-1-85	

CLOCKED COLOR BAR
PRINTED CIRCUIT BOARD ASSEMBLY

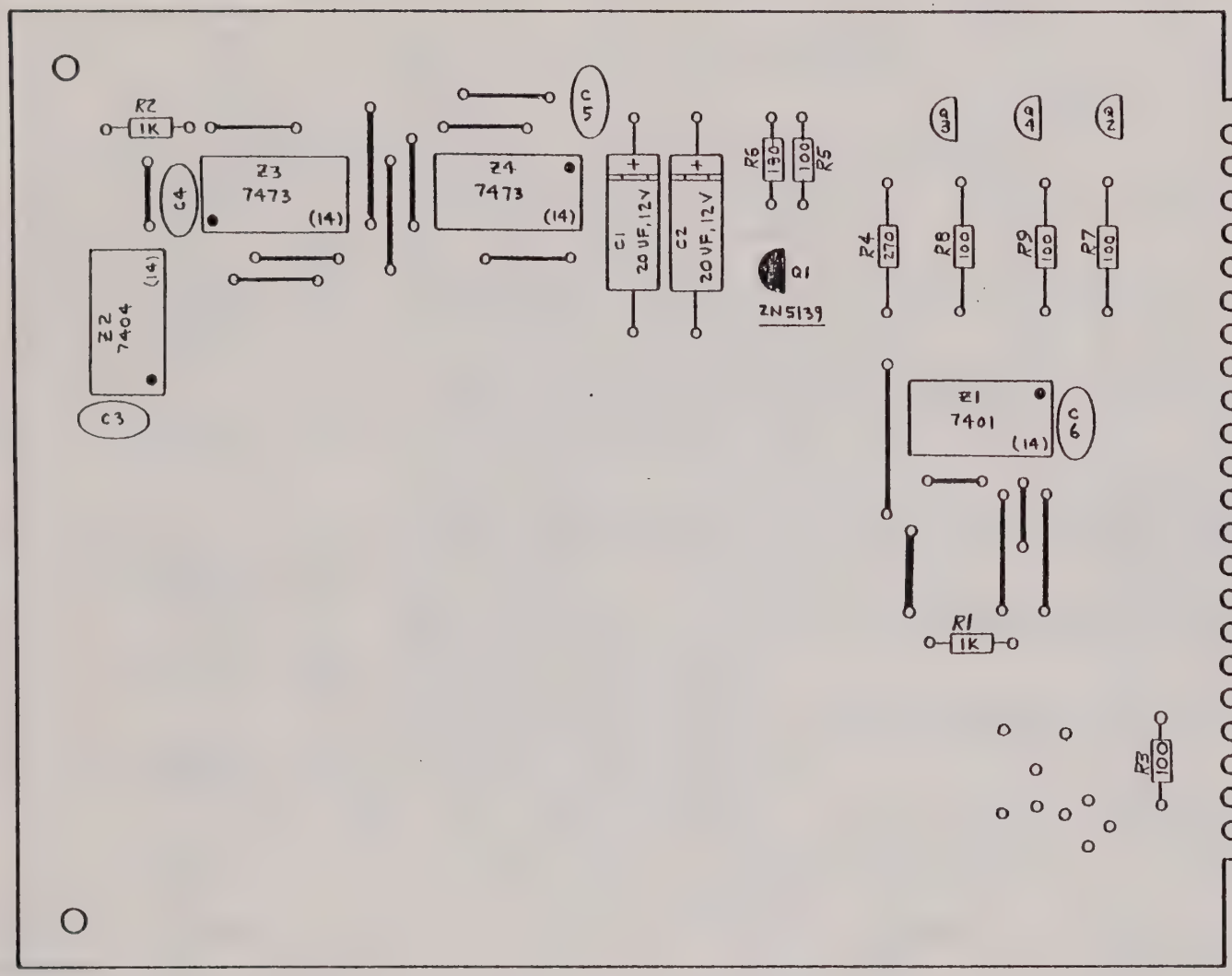
PARTS LIST PL-4008

ARTWORK REV. A (10/84) 2/11/85 SHT 1 OF 1

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	QTY/GROUP 2	MFR.	Vii DWG.NO.
PCB ASSEMBLY		x	x	Vii	L-4008
PCB ARTWORK	COND. SIDE	x	x	Vii	CB-4008
PCB ARTWORK	COMP. SIDE	x	x	Vii	CF-NONE
PCB SCHEMATIC		x	x	Vii	S-4008
Hole Count		130	139		
Transistor	2N5134	3	3	BAS	A-1844
"	2N5139	1	1	BAS	A-1845
"	2N3646	x	1	BAS	A-1858
Resistor, Fixed	100 ohms	5	5	BAS	A-1450
"	180 ohms	1	1	BAS	A-1450
"	270 ohms	1	1	BAS	A-1450
"	1K ohms	2	2	BAS	A-1450
"	1.5K ohms	x	1	BAS	A-1450
"	12K ohms	x	1	BAS	A-1450
Capacitor	0.1uf, 10v	4	4	BAS	A-1455
"	20uf, 12v	2	2	BAS	A-1458
"	27 pf	x	1	BAS	A-1454
I.C. Socket	14 pin	4	4	BAS	A-1465
I.C.	7401	1	1	BAS	
"	7404	1	1	BAS	
"	7473	2	2	BAS	
Bus wire, jumper	#22 Awg Solid	16	16	BAS	

CLOCKED COLOR BAR REV. A (10-84) DWG. NO. L-4008 (GROUP 1)

PARTS LIST
2-11-85



Z	+5V
Y	GND (SHIELD)
X	RESOLUTION (G) OUT
W	GND (SHIELD)
V	RESOLUTION (R) OUT
U	GND (SHIELD)
T	RESOLUTION (B) OUT
S	GND
R	RESOLUTION IN
P	GND
N	GREEN OUT
M	BLUE OUT
L	RED OUT
K	-5V
J	+H BLANK IN
H	20 H CLOCK IN
F	COLOR BAR ON
E	+5V
D	---
C	---
B	PATTERN BUSS
A	GND

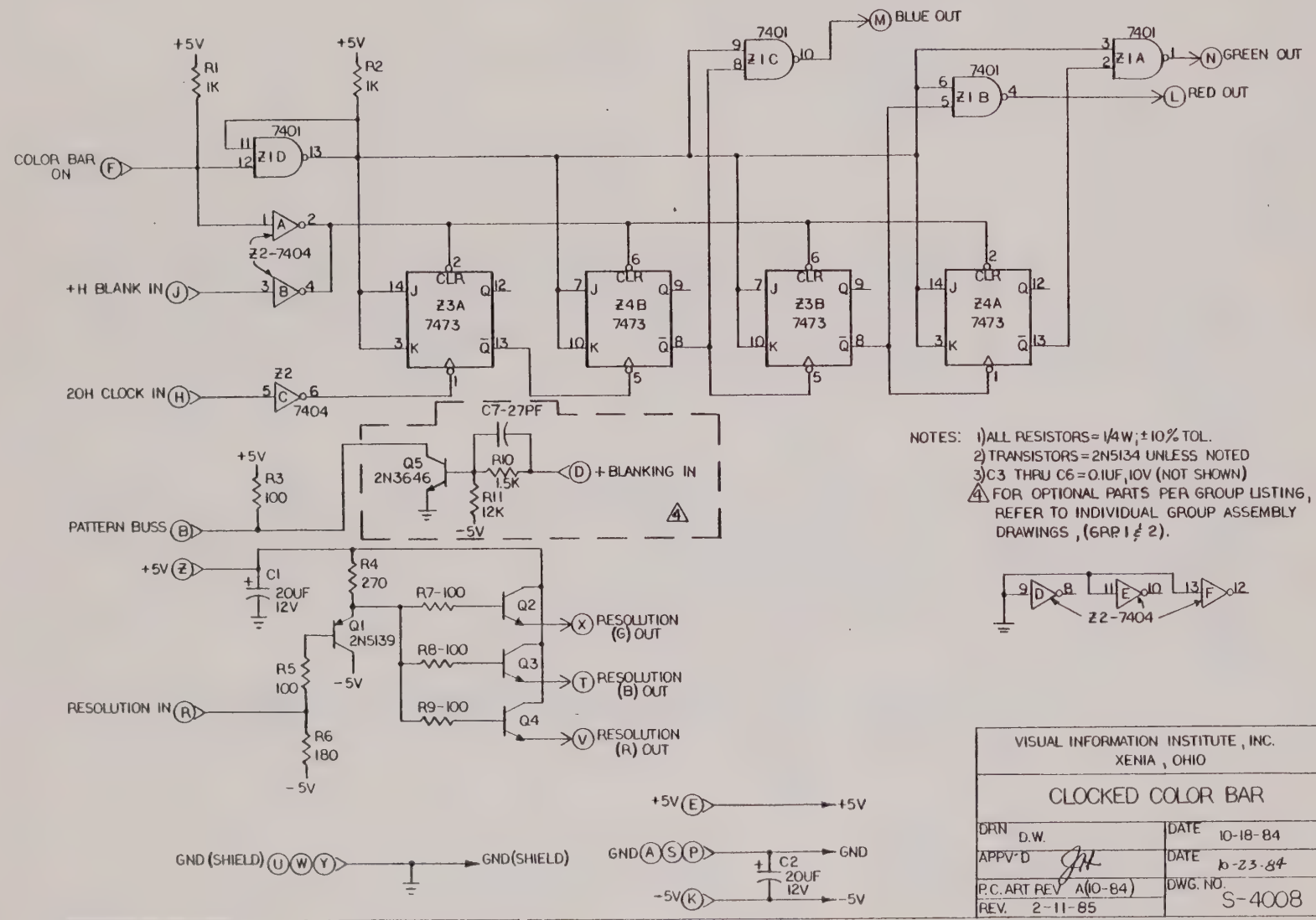
NO. HOLES/BOARD=130

NOTES: 1) TRANS = 2N5134, UNLESS NOTED.
2) ALL RESISTORS = 1/4W; ±10% TOL.
3) C3 THRU C6 = 0.1UF, 10V.
4) O—O BUS WIRE, #22 AWG SOLID.

POSITION 6C 4008 CLOCKED COLOR BAR (Group 1)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
Y	GROUND	(TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B)(CLOCKED COLOR BAR, PINS W, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
X	RESOLUTION B OUT .	(TTL VIDEO (5C), PIN W)
W	GROUND	(TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B)(CLOCKED COLOR BAR, PINS Y, U, S, P) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
V	RESOLUTION G OUT .	(TTL VIDEO (4C), PIN W)
U	GROUND	(CLOCKED COLOR BAR, PINS Y, W, S, P)(TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
T	RESOLUTION R OUT .	(TTL VIDEO (3C), PIN W)
S	GROUND	(CLOCKED COLOR BAR, PINS Y, W, U, P)(TTL VIDEO (3C,4C,5C) PINS X, V, N, F, B) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
R	RESOLUTION IN . .	(RESOLUTION (7C), PIN D)(CHARACTER, PIN C)
P	GROUND	(CLOCKED COLOR BAR, PINS Y, W, U, S)(TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B) (RESOLUTION (7C), PINS C, E, H, K, L)(CHARACTER, PINS B, D, R)(GROUND BUSS)
N	GREEN OUT	(TTL VIDEO (4C), PIN Y)
M	BLUE OUT	(TTL VIDEO (5C), PIN Y)
L	RED OUT	(TTL VIDEO (3C), PIN Y)
K	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
J	+H BLANK IN	(GRAY SCALE SELECT, PIN D)(VIDEO CLOCK, PIN F)(CLOCKED BAR/DOT, PIN D) (CHARACTER, PIN X)(uP INTERFACE (P1), PIN 4)
H	20H CLOCK IN . . .	(GRAY SCALE SELECT, PIN E)(uP INTERFACE (P1), PIN R)
F	COLOR BAR ON . . .	(PATTERN LOGIC, PIN P)
E	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
D	--	
C	--	
B	PATTERN IN	(TTL VIDEO (3C,4C,5C), PIN P)(GRAY SCALE, PIN L)(VIDEO CLOCK, PIN R) (CLOCKED BAR/DOT, PIN U)(PATTERN LOGIC, PIN Z)
A	--	



VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
CLOCKED COLOR BAR	
DRN D.W.	DATE 10-18-84
APPV'D	DATE 10-23-84
P.C. ART REV A(10-84)	DWG. NO. S-4008
REV. 2-11-85	

RESOLUTION
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-4013

ARTWORK REV. A (9/84) 10/23/84 SHT 1 OF 2

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	QTY/GROUP 2	MFR.	Vii DWG.NO.
PCB ASSEMBLY		x	x	Vii	L-4013
PCB ARTWORK	COND. SIDE	x	x	Vii	CB-4013
PCB ARTWORK	COMP. SIDE	x	x	Vii	CF-NONE
PCB SCHEMATIC		x	x	Vii	S-4013
Hole Count		182	141		
Diodes	1N4154	3	3	BAS	A-1797
Transistors	2N2369	5	5	BAS	
"	2N4036	1	1	BAS	A-1862
"	2N5134	8	3	BAS	A-1844
"	2N5139	4	4	BAS	A-1845
Resistors, Fixed	10 ohm	6	6	BAS	A-1450
"	100 ohm	4	4	BAS	A-1450
"	120 ohm	2	2	BAS	A-1450
"	270 ohm	2	3	BAS	A-1450
"	330 ohm	1	1	BAS	A-1450
"	470 ohm	2	2	BAS	A-1450
"	1K ohm	4	5	BAS	A-1450
"	2.7K ohm	4	4	BAS	A-1450
"	4.7K ohm	5	x	BAS	A-1450
"	18K ohm	8	3	BAS	A-1450
Resistors, Var.	5K ohm	5	1	BAS	A-1460
"	500 ohm	1	1	BAS	A-1460
Capacitors	0.01uf, 100v	5	5	BAS	
"	2uf, 25v	1	1	BAS	A-1458
"	20uf, 12v	2	2	BAS	A-1458
Bus wire, jumper	#22 Awg Solid	4	5	BAS	

RESOLUTION
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-4013

ARTWORK REV. A (9/84) 10/23/84 SHT 2 OF 2

GENERAL CALIBRATION

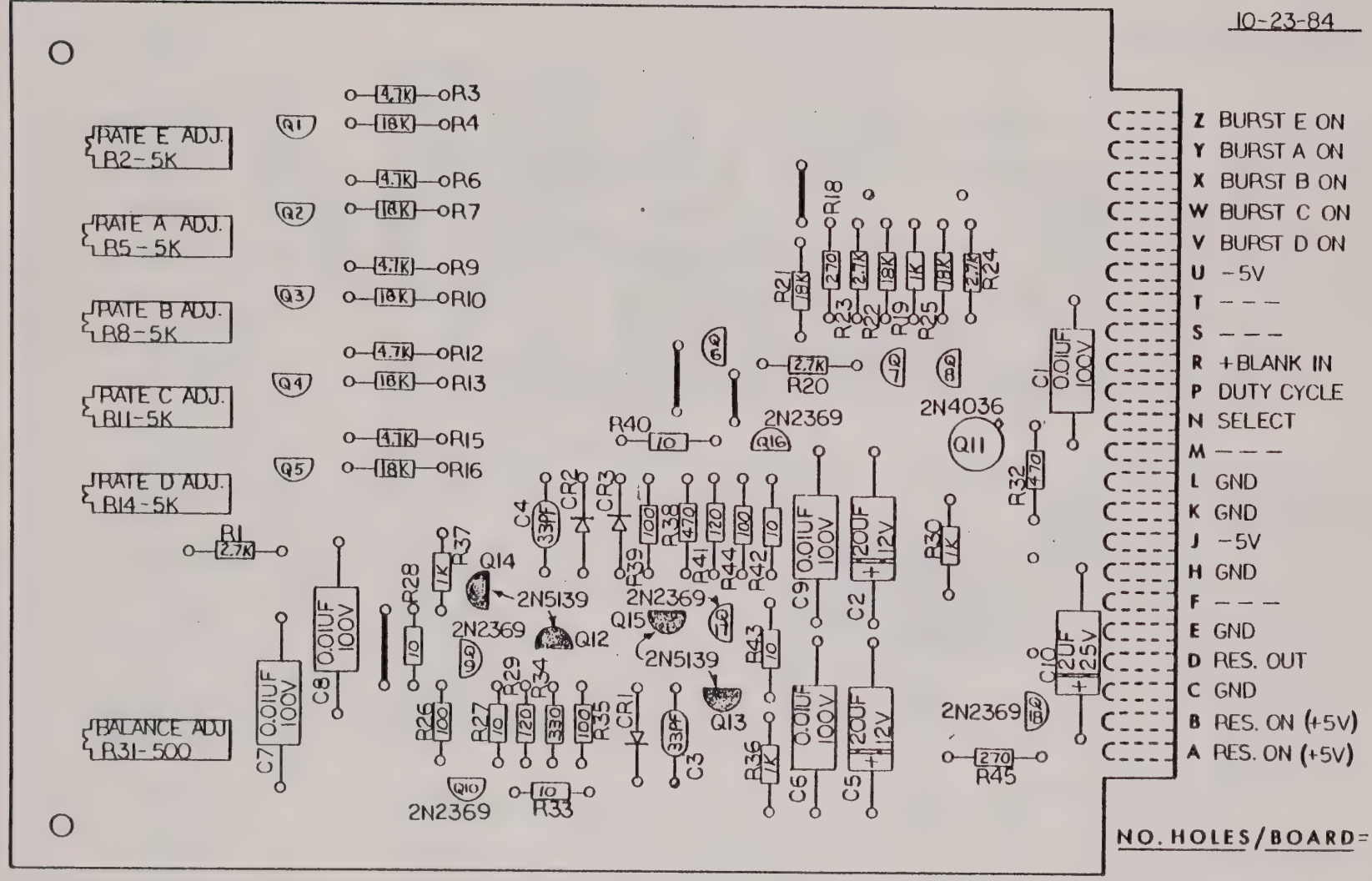
GROUP	RESOLUTION RANGE						SUGGESTED TIMING CAPACITOR VALUE C3 & C4
		A	B	C	D	E	
1	mHz	10	15	20	25	30	33 pf
	nsec/cycle	100	67	50	40	36	

GROUP	APPLICATION	SUGGESTED TIMING CAPACITOR VALUE C3 & C4
2	Character Clock – Value of C3 and C4 plus nominal range of adjustment.	47 pf

RESOLUTION

REV. A (9-84) DWG. NO. L-4013 (GROUP I)

PARTS LIST
10-23-84



NO. HOLES/BOARD=182

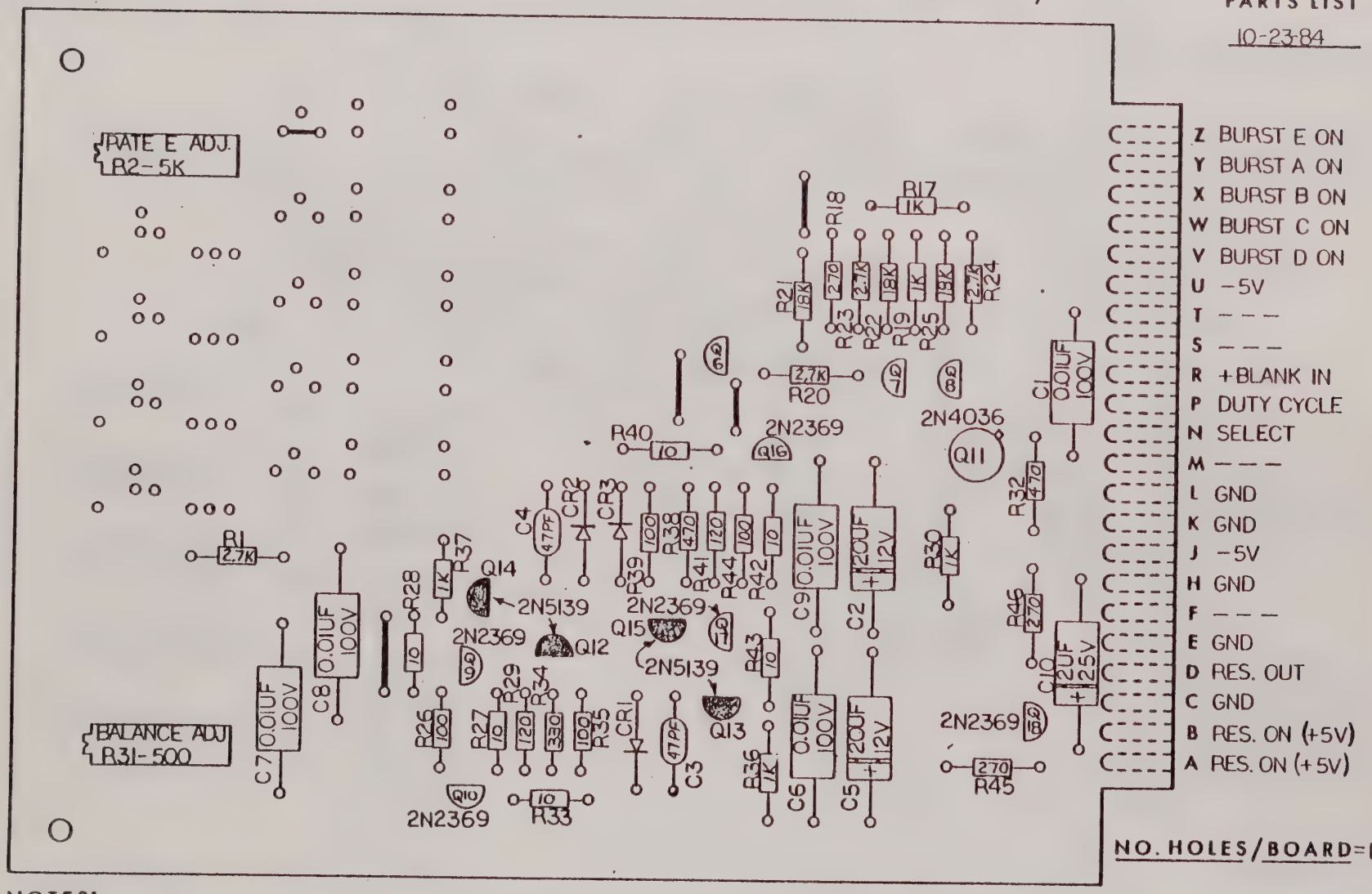
NOTES:
1) ALL RESISTORS = 1/4W; ±10% TOL.
2) ALL DIODES = IN4154
3) ALL TRANSISTORS = 2N5134, UNLESS NOTED.
4) o——o = BUS WIRE, #22 AWG, SOLID.

RESOLUTION

REV. A (9-84) DWG. NO. L-4013 (GROUP 2)

PARTS LIST

10-23-84



NO. HOLES/BOARD=141

NOTES:

1) ALL RESISTORS = 1/4W; ±10% TOL.
2) ALL DIODES = IN4154
3) ALL TRANSISTORS = 2N5134, UNLESS NOTED.
4) o—o = BUS WIRE, * 22 AWG, SOLID.

POSITION 7C 4013 RESOLUTION (Group 1)

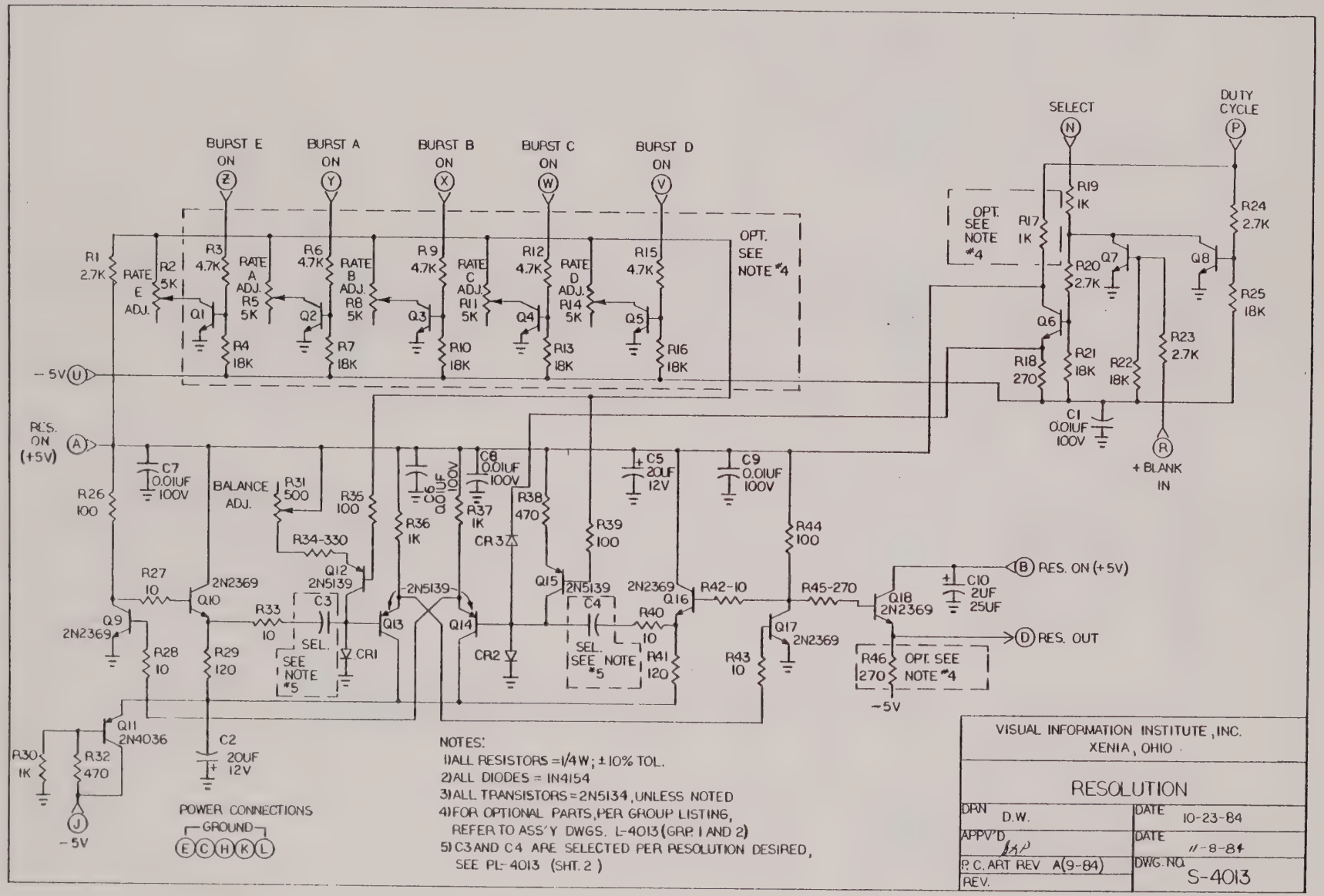
MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	BURST 1	(RESOLUTION CONTROL, PIN R)
Y	BURST 2	(RESOLUTION CONTROL, PIN N)
X	BURST 3	(RESOLUTION CONTROL, PIN K)
W	BURST 4	(RESOLUTION CONTROL, PIN H)
V	BURST 5	(RESOLUTION CONTROL, PIN E)
U	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
T	--	
S	--	
R	+BLANK IN	(CHARACTER, PIN Z)(RESOLUTION (9C), PIN R)(PULSE OUTPUT, PIN D) (TTL PULSE OUTPUT, PIN D)(CLOCKED BAR/DOT, PIN J)(RESOLUTION CONTROL, PIN C) (uP INTERFACE (P1), PIN 6)
P	DUTY CYCLE IN . .	(RESOLUTION CONTROL, PIN A)
N	RESOLUTION ON . .	(+5v. BUSS)(POWER REGULATOR, PIN C)
M	--	
L	GROUND	(RESOLUTION (7C), PINS K, H, E, C)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B)(GROUND BUSS)
K	GROUND	(RESOLUTION (7C), PINS L, H, E, C)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B)(GROUND BUSS)
J	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
H	GROUND	(RESOLUTION (7C), PINS K, L, E, C)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B)(GROUND BUSS)
F	--	
E	GROUND	(RESOLUTION (7C), PINS K, L, H, C)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B)(GROUND BUSS)
D	OUTPUT	(CLOCKED COLOR BAR, PIN R)(CHARACTER, PIN C)
C	GROUND	(RESOLUTION (7C), PINS L, K, H, E)(CLOCKED COLOR BAR, PINS Y, W, U, S, P) (TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B)(GROUND BUSS)
B	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
A	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)

POSITION 9C 4013 RESOLUTION (Character Cx) (Group 2)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	--	
Y	--	
X	--	
W	--	
V	--	
U	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
T	--	
S	--	
R	+BLANK IN	(CHARACTER, PIN Z)(RESOLUTION (7C), PIN R)(PULSE OUTPUT, PIN D) (TTL PULSE OUTPUT, PIN D)(CLOCKED BAR/DOT, PIN J)(RESOLUTION CONTROL, PIN C) (uP INTERFACE (P1), PIN 6)
P	CONTROL	(CHARACTER, PIN T)(CONTROL PANEL, S3, FUNCTION SELECT - CHARACTER)
N	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
M	--	
L	GROUND	(RESOLUTION (9C), PINS K, H, E, C)(GROUND BUSS)
K	GROUND	(RESOLUTION (9C), PINS L, H, E, C)(GROUND BUSS)
J	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
H	GROUND	(RESOLUTION (9C), PINS L, K, E, C)(GROUND BUSS)
F	--	
E	GROUND	(RESOLUTION (9C), PINS L, K, H, C)(GROUND BUSS)
D	CLOCK OUT	(CHARACTER, PIN Y)
C	GROUND	(RESOLUTION (9C), PINS L, K, H, E)(GROUND BUSS)
B	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
A	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)



NOTES:
1) ALL RESISTORS = 1/4W; ± 10% TOL.
2) ALL DIODES = IN4154
3) ALL TRANSISTORS = 2N5134, UNLESS NOTED
4) FOR OPTIONAL PARTS, PER GROUP LISTING, REFER TO ASS'Y DWGS. L-4013 (GRP. 1 AND 2)
5) C3 AND C4 ARE SELECTED PER RESOLUTION DESIRED, SEE PL-4013 (SHT. 2)

VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
RESOLUTION	
DRN D.W.	DATE 10-23-84
APPV'D	DATE 11-8-84
P.C. ART REV A(9-84)	DWG. NO. S-4013
REV.	

CHARACTER
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-4014

ARTWORK REV. A (8/84) 11/1/84 SHT 1 OF 2

DESCRIPTION	VALUE/TYPE	QTY/GROUP 0	MFR.	Vii DWG.NO.
PCB ASSEMBLY		x	Vii	L-4014
PCB ARTWORK	COND. SIDE	x	Vii	CB-4014
PCB ARTWORK	COMP. SIDE	x	Vii	CF-NONE
PCB SCHEMATIC		x	Vii	S-4014
Hole Count		273		
Transistor	2N2369	1	BAS	A-1844
Resistor, Fixed	270 ohms	1	BAS	A-1450
"	470 ohms	3	BAS	A-1450
"	1K ohms	13	BAS	A-1450
Resistor Network	1K (10 pin)	2	BAS	A-1873
Capacitor	0.1uf, 10v	9	BAS	A-1456
"	20uf, 12v	1	BAS	A-1458
I.C. Socket	14 pin	6	BAS	A-1465
"	16 pin	4	BAS	A-1465
I.C.	7400	1	BAS	
"	7405	1	BAS	
"	74S20	1	BAS	
"	74S86	1	BAS	
"	74S188	1	BAS	
"	74LS74	1	BAS	
"	74LS132	1	BAS	
"	74LS161	2	BAS	
"	74LS166	1	BAS	
Bus wire, jumper	#22 Awg solid	24		

CHARACTER
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-4014

ARTWORK REV. A (8/84) 11/1/84 SHT 2 OF 2

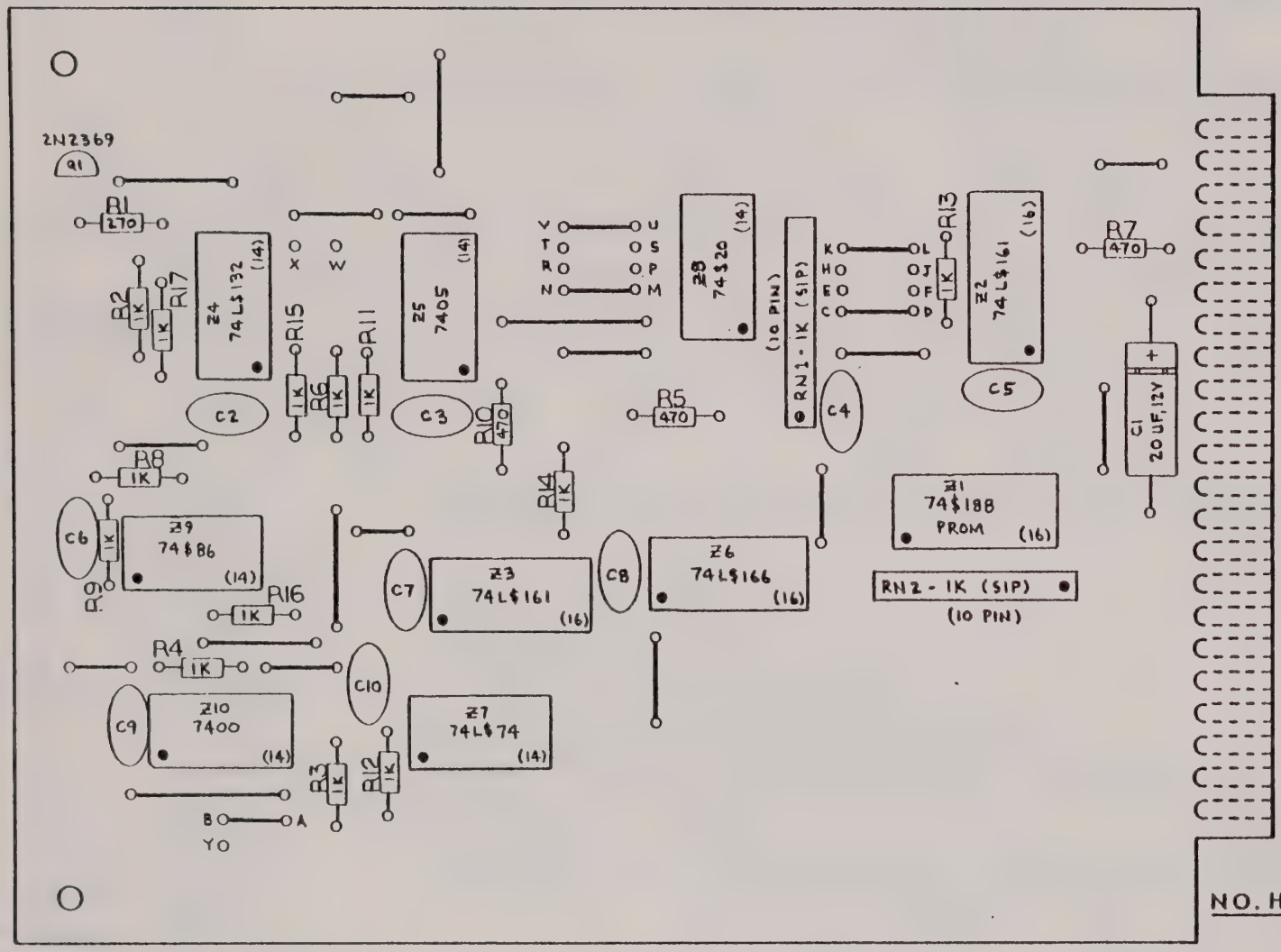
JUMPER USAGE FOR DESIRED CHARACTER

DESCRIPTION	VALUE	JUMPERS USED
CHARACTER [x]	10 x 10 matrix	C-D, K-L, M-N, U-V

CHARACTER 8-84 REV. A DWG. NO. L-4014 (GROUP 0)

PARTS LIST

11-1-84



NO. HOLES/BOARD = 273

NOTES: 1) ALL RESISTORS = 1/4 W; ± 10 % TOL.

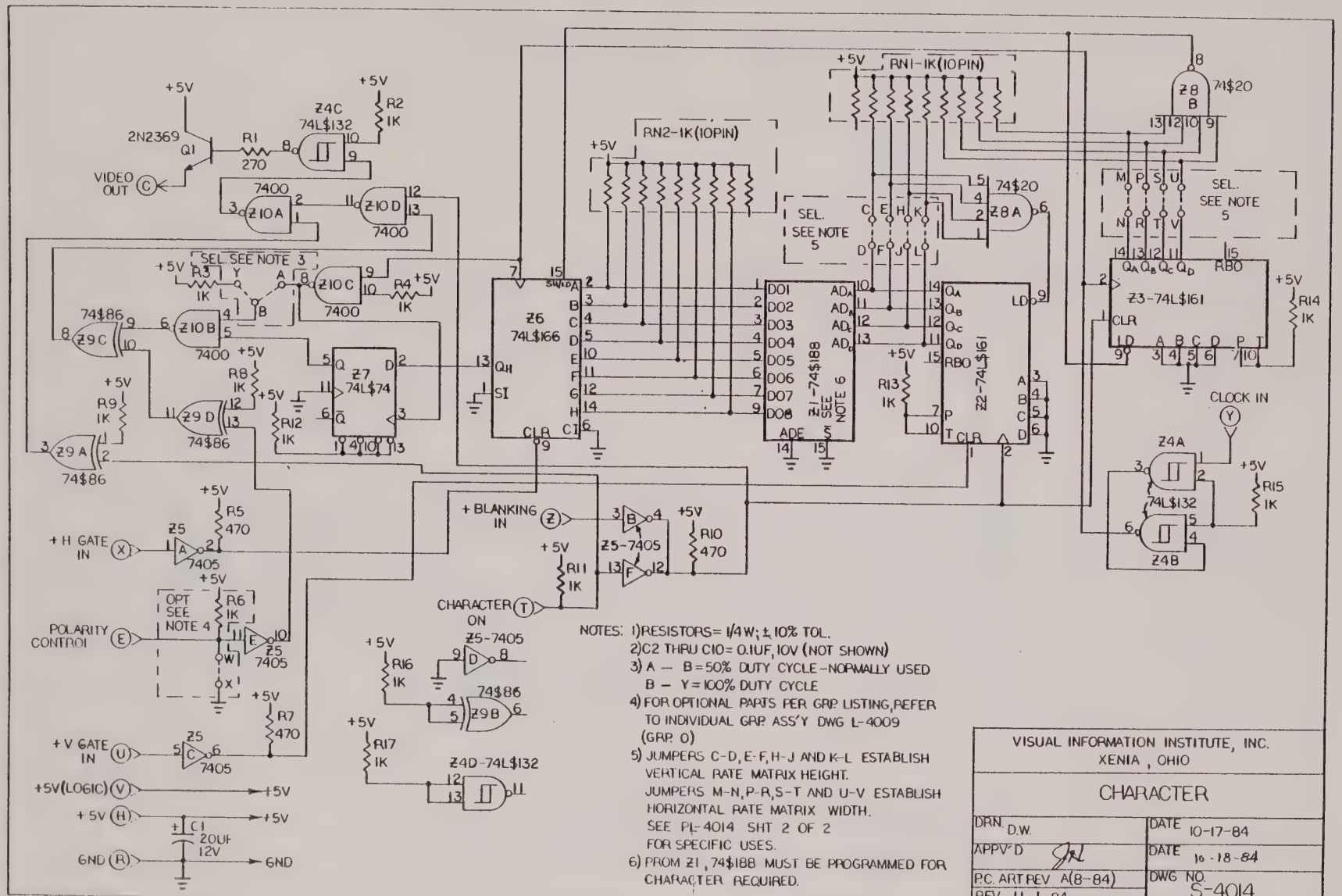
2) C2 THRU C10 = 0.1 UF, 10 V.

3) o—o BUS WIRE, # 22 AWG. SOLID

POSITION 8C 4014 CHARACTER (Group 0)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	+BLANK IN	(RESOLUTION (7C,9C), PIN R)(PULSE OUTPUT, PIN D)(TTL PULSE OUTPUT, PIN D) (CLOCKED BAR/DOT, PIN J)(RESOLUTION CONTROL, PIN C)(uP INTERFACE (P1), PIN 6)
Y	CLOCK IN	(RESOLUTION (9C), PIN D)
X	+H GATE	(CLOCKED COLOR BAR, PIN J)(GRAY SCALE SELECT, PIN D)(VIDEO CLOCK, PIN F) (CLOCKED BAR/DOT, PIN D)(uP INTERFACE (P1), PIN 4)
W	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
V	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
U	+V GATE	(PULSE OUTPUT, PIN C)(uP INTERFACE (P1), PIN 7)
T	CHARACTER ON . . .	(RESOLUTION (9C), PIN P)
S	--	
R	GROUND	(CHARACTER, PINS D, B)(RESOLUTION (7C), PINS C, E, H, K, L)(GROUND BUSS) (CLOCKED COLOR BAR, PINS Y, W, U, S, P)(TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B)
P	--	
N	--	
M	--	
L	--	
K	--	
J	--	
H	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
F	--	
E	--	
D	GROUND	(CHARACTER, PINS R, B)(RESOLUTION (7C), PINS C, E, H, K, L)(GROUND BUSS) (CLOCKED COLOR BAR, PINS Y, W, U, S, P)(TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B)
C	OUTPUT	(RESOLUTION (7C), PIN D)(CLOCKED COLOR BAR, PIN R)
B	GROUND	(CHARACTER, PINS R, D)(RESOLUTION (7C), PINS C, E, H, K, L)(GROUND BUSS) (CLOCKED COLOR BAR, PINS Y, W, U, S, P)(TTL VIDEO (3C,4C,5C), PINS X, V, N, F, B)
A	--	



NOTES:
1) RESISTORS = 1/4 W; ± 10% TOL.
2) C2 THRU C10 = 0.1UF, 10V (NOT SHOWN)
3) A — B = 50% DUTY CYCLE — NORMALLY USED
   B — Y = 100% DUTY CYCLE
4) FOR OPTIONAL PARTS PER GRP LISTING, REFER TO INDIVIDUAL GRP ASS'Y DWG L-4009 (GRP 0)
5) JUMPERS C-D, E-F, H-J AND K-L ESTABLISH VERTICAL RATE MATRIX HEIGHT.
   JUMPERS M-N, P-R, S-T AND U-V ESTABLISH HORIZONTAL RATE MATRIX WIDTH.
   SEE PL-4014 SHT 2 OF 2 FOR SPECIFIC USES.
6) PROM Z1, 74$188 MUST BE PROGRAMMED FOR CHARACTER REQUIRED.

VISUAL INFORMATION INSTITUTE, INC.
XENIA, OHIO

CHARACTER

DRN. D.W.	DATE 10-17-84
APPV'D	DATE 10-18-84
P.C. ART REV A(8-84)	DWG NO. S-4014
REV. 11-1-84	

PULSE OUTPUT
PRINTED CIRCUIT BOARD ASSEMBLY

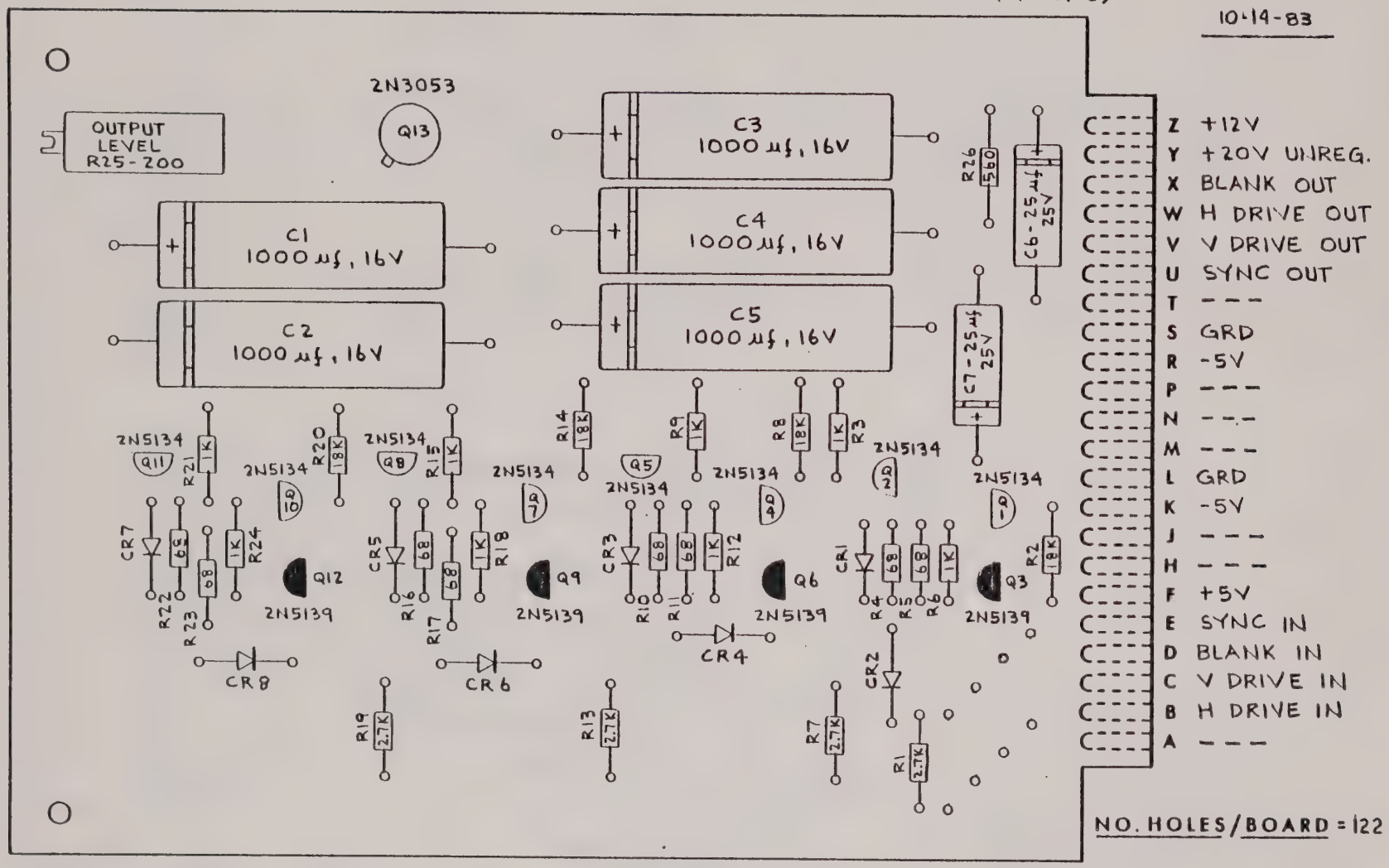
PARTS LIST PL-2003

ARTWORK REV. D (11/80) 10/14/83 SHT 1 OF 1

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	2	3	MFR.	Vii DWG. NO.
P.C.B. ASSEMBLY		x	x	x	Vii	L-2003
P.C.B. ARTWORK	CONDUCT SIDE	x	x	x	Vii	CB-2003
P.C.B. ARTWORK	COMP. SIDE	x	x	x	Vii	CF-NONE
P.C.B. SCHEMATIC		x	x	x	Vii	S-2003
Diode	1N4154	8	8	8	BAS	A-1797
Transistor	2N3053	1	1	1	BAS	A-1834
"	2N5134	8	8	8	BAS	A-1844
"	2N5139	4	4	4	BAS	A-1845
Resistor, Fixed	68 ohms	8	8	8	BAS	A-1450
"	560 ohms	1	1	1	BAS	A-1450
"	1K ohms	8	12	8	BAS	A-1450
"	2.7K ohms	4	4	4	BAS	A-1450
"	18K ohms	4	4	4	BAS	A-1450
"	470 ohms	x	x	4	BAS	A-1450
Resistor, Var.	200 ohms	1	1	1	BAS	A-1460
Capacitor	25 uf, 25v	2	2	2	BAS	A-1458
"	1000 uf, 16v	5	5	5	BAS	A-1459

PULSE OUTPUT 11-80 REV. D DWG. NO. L-2003 (GROUP 1)

PARTS LIST
10-14-83



NO. HOLES/BOARD = 122

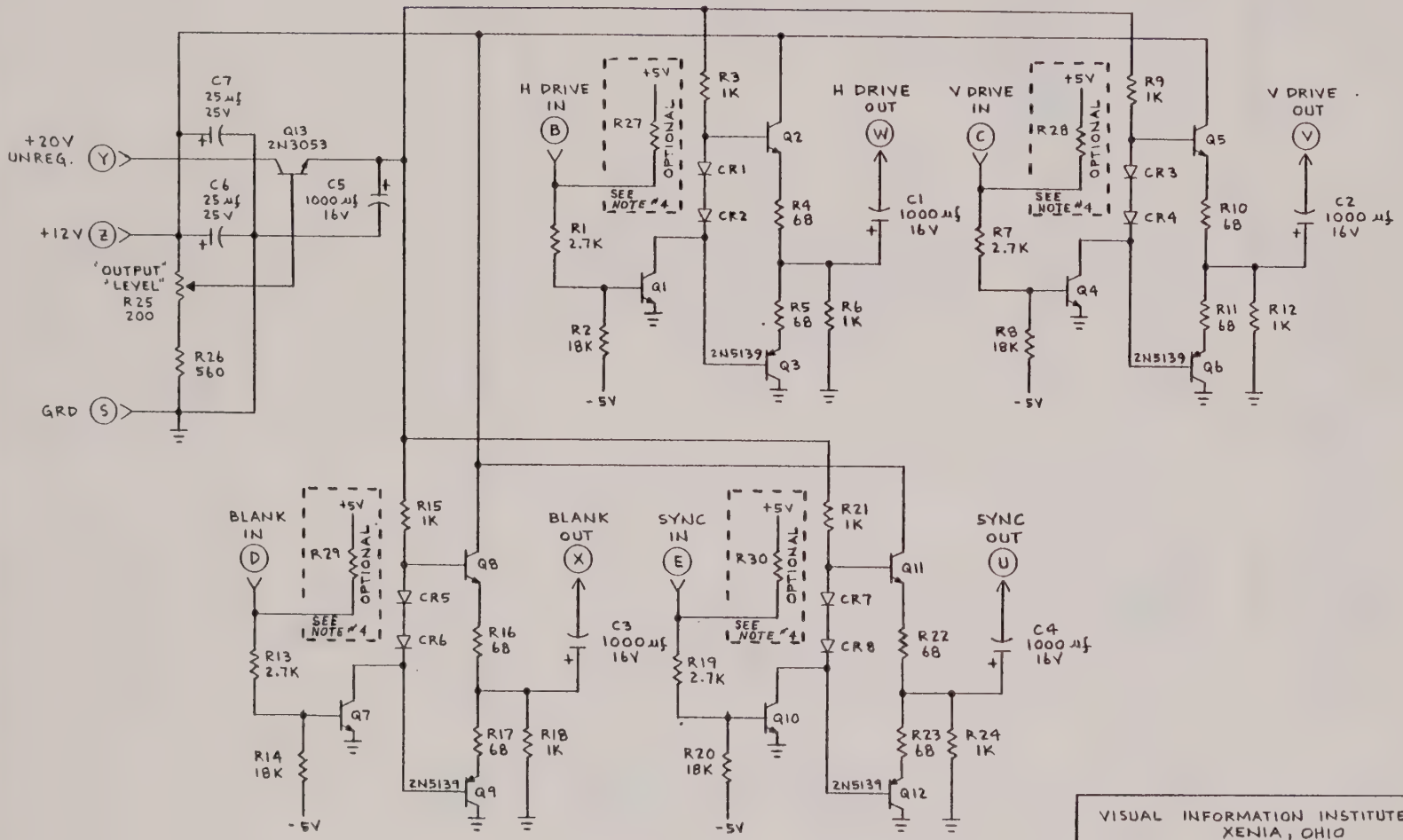
NOTES: 1) ALL DIODES = IN4154.

2) ALL RESISTORS = 1/4 W, ± 10 % TOL.

POSITION 11C 2003 PULSE OUTPUT (Group 1)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	+12v.	(+12v. BUSS)(POWER REGULATOR, PIN Y)
Y	+D.C.	(POWER REGULATOR, PIN J)
X	BLANK OUT	(CONTROL PANEL, TP3, BLANKING)
W	H DRIVE OUT	(CONTROL PANEL, TP1, H DRIVE)
V	V DRIVE OUT	(CONTROL PANEL, TP2, V DRIVE)
U	SYNC OUT	(CONTROL PANEL, TP4, SYNC)
T	--	
S	GROUND	(PULSE OUTPUT, PIN L)(GROUND BUSS)
R	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
P	--	
N	--	
M	--	
L	GROUND	(PULSE OUTPUT, PIN S)(GROUND BUSS)
K	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
J	--	
H	--	
F	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
E	+SYNC IN	(TTL PULSE OUTPUT, PIN E)(VIDEO CONTROL, PIN A)(uP INTERFACE (P1), PIN 3)
D	+BLANK IN	(TTL PULSE OUTPUT, PIN D)(RESOLUTION (7C,9C), PIN R)(CHARACTER, PIN Z) (CLOCKED BAR/DOT, PIN J)(RESOLUTION CONTROL, PIN C)(uP INTERFACE (P1), PIN 6)
C	+V TRIG IN	(uP INTERFACE (P1), PIN 8)
B	+H TRIG IN	(uP INTERFACE (P1), PIN B)
A	--	



POWER CONNECTIONS

+5V	-5V	GRD
F	K R	L

NOTES:

1) ALL DIODES = 1N4154
2) ALL TRANSISTORS = 2N5134, UNLESS NOTED.
3) ALL RESISTORS = 1/4W, ± 10% TOL.
4) FOR OPTIONAL PARTS SEE GROUP LISTINGS, PL-2003 AND L-2003.

VISUAL INFORMATION INSTITUTE, INC.
XENIA, OHIO

PULSE OUTPUT

DRN PAT ANTONICK	DATE 7-22-80
APPV'D. [signature]	DATE 7-25-80
P.C. ART REV. D [11-80]	S-2003
REV. 10-14-83	

TTL PULSE OUTPUT
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-2118

ARTWORK REV. C (8/83) 4/26/84 SHT 1 OF 3

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	2	3	4	5	MFR.	Vii DWG. NO.
PCB ASSEMBLY		x	x	x	x	x	Vii	L-2118
PCB ARTWORK	CONDUCT SIDE	x	x	x	x	x	Vii	CB-2118
PCB ARTWORK	COMP. SIDE	x	x	x	x	x	Vii	CF-NONE
PCB SCHEMATIC		x	x	x	x	x	Vii	S-2118
Transistor	2N5134	6	4	6	4	6	BAS	A-1844
Resistor, Fixed	56 ohms	6	4	6	4	6	BAS	A-1450
"	1K ohms	21	12	25	16	19	BAS	A-1450
"	4.7K ohms	6	4	6	4	6	BAS	A-1450
"	10K ohms	6	4	6	4	6	BAS	A-1450
"	18K ohms	6	4	6	4	6	BAS	A-1450
Capacitor	0.1uf, 10v	8	5	8	5	8	BAS	A-1455
"	20uf, 12v	2	2	2	2	2	BAS	A-1458
I.C.	7403	3	2	3	2	3	BAS	A-1748
"	7404	3	2	3	2	3	BAS	
"	74128	2	1	2	1	2	BAS	
"	7428	x	x	x	x	x	BAS	
"	7433	x	x	x	x	x	BAS	
I.C. Socket	14 pin	8	5	8	5	8	BAS	A-1465
Bus Wire, Jumper	#24 Awg Sld	22	17	22	17	22	BAS	

TTL PULSE OUTPUT
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-2118

ARTWORK REV. C (3/83) 4/26/84 SHT 2 OF 3

DESCRIPTION	VALUE/TYPE	QTY/GROUP 11	12	13	14	15	MFR.	Vii DWG. NO.
PCB ASSEMBLY		x	x	x	x	x	Vii	L-2118
PCB ARTWORK	CONDUCT SIDE	x	x	x	x	x	Vii	CB-2118
PCB ARTWORK	COMP. SIDE	x	x	x	x	x	Vii	CF-NONE
PCB SCHEMATIC		x	x	x	x	x	Vii	S-2118
Transistor	2N5134	6	4	6	4	6	BAS	A-1844
Resistor, Fixed	56 ohms	x	x	x	x	x	BAS	A-1450
"	1K ohms	21	12	25	16	19	BAS	A-1450
"	4.7K ohms	6	4	6	4	6	BAS	A-1450
"	10K ohms	x	x	x	x	x	BAS	A-1450
"	18K ohms	6	4	6	4	6	BAS	A-1450
Capacitor	0.1uf, 10v	8	5	8	5	8	BAS	A-1455
"	20uf, 12v	2	2	2	2	2	BAS	A-1458
I.C.	7403	3	2	3	2	3	BAS	A-1748
"	7404	3	2	3	2	3	BAS	
"	74128	x	x	x	x	x	BAS	
"	7428	2	1	2	1	2	BAS	
"	7433	x	x	x	x	x	BAS	
I.C. Socket	14 pin	8	5	8	5	8	BAS	A-1465
Bus Wire, Jumper	#24 Awg Sld	28	21	28	21	28	BAS	

TTL PULSE OUTPUT
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-2118

ARTWORK REV. C (3/83) 4/26/84 SHT 3 OF 3

DESCRIPTION	VALUE/TYPE	QTY/GROUP 21	22	23	24	25	MFR.	Vii DWG. NO.
PCB ASSEMBLY		x	x	x	x	x	Vii	L-2118
PCB ARTWORK	CONDUCT SIDE	x	x	x	x	x	Vii	CB-2118
PCB ARTWORK	COMP. SIDE	x	x	x	x	x	Vii	CF-NONE
PCB SCHEMATIC		x	x	x	x	x	Vii	S-2118
Transistor	2N5134	6	4	6	4	6	BAS	A-1844
Resistor, Fixed	56 ohms	x	x	x	x	x	BAS	A-1450
"	1K ohms	21	12	25	16	19	BAS	A-1450
"	4.7K ohms	6	4	6	4	6	BAS	A-1450
"	10K ohms	x	x	x	x	x	BAS	A-1450
"	18K ohms	6	4	6	4	6	BAS	A-1450
Capacitor	0.1uf, 10v	8	5	8	5	8	BAS	A-1455
"	20uf, 12v	2	2	2	2	2	BAS	A-1458
I.C.	7403	3	2	3	2	3	BAS	A-1748
"	7404	3	2	3	2	3	BAS	
"	74128	x	x	x	x	x	BAS	
"	7428	x	x	x	x	x	BAS	
"	7433	2	1	2	1	2	BAS	
I.C. Socket	14 pin	8	5	8	5	8	BAS	A-1465
Bus Wire, Jumper	#24 Awg Sld	28	21	28	21	28	BAS	

Z5 AND Z8 SELECTION

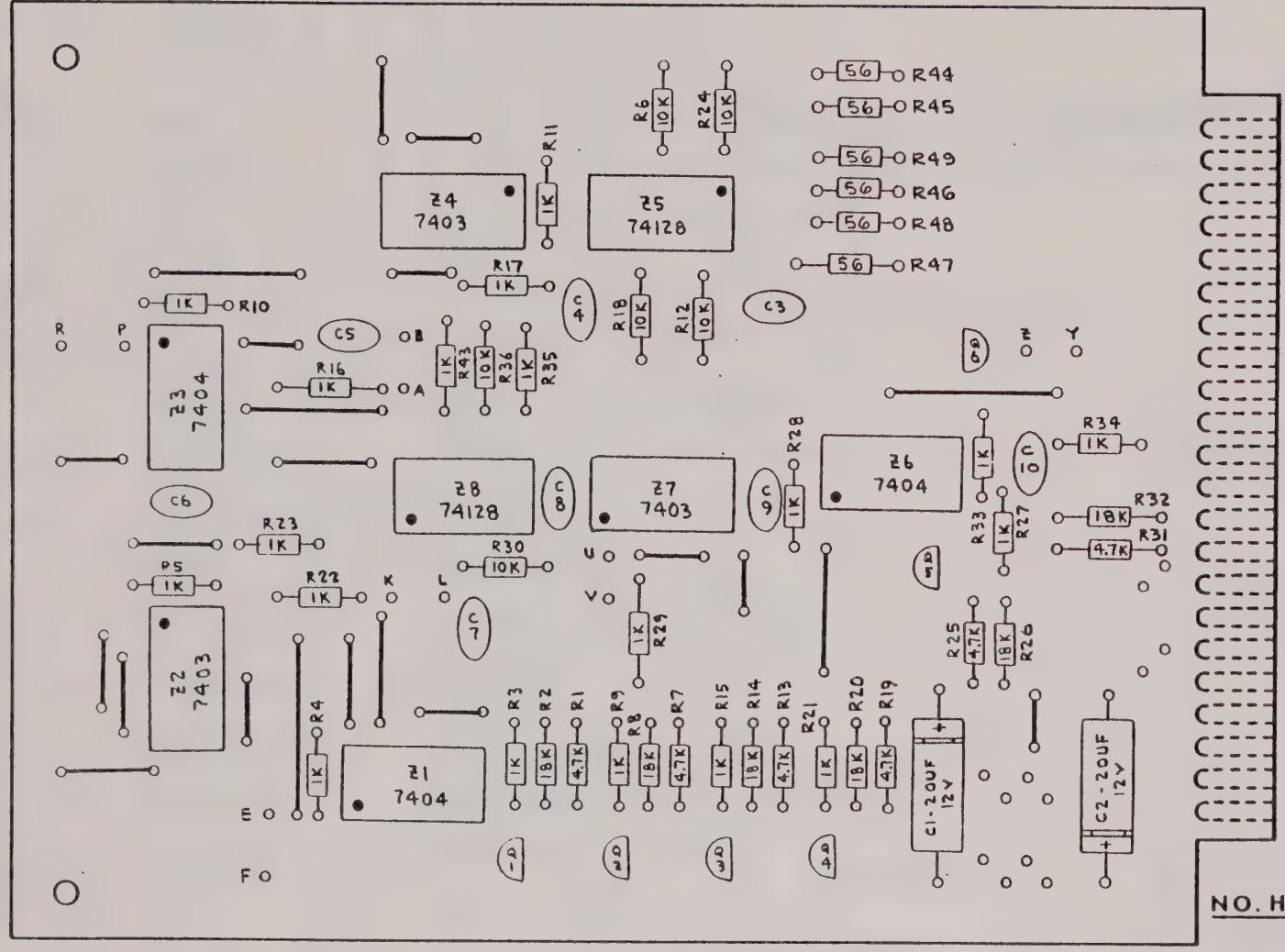
74128 . . . For line driver output which provides a 50 ohm source impedance.

7428 . . . For conventional TTL output.

7433 . . . For open collector output.

TTL PULSE OUTPUT 3-83 REV.C DWG. NO. L-2118 (GROUP 5)

PARTS LIST
4-26-84



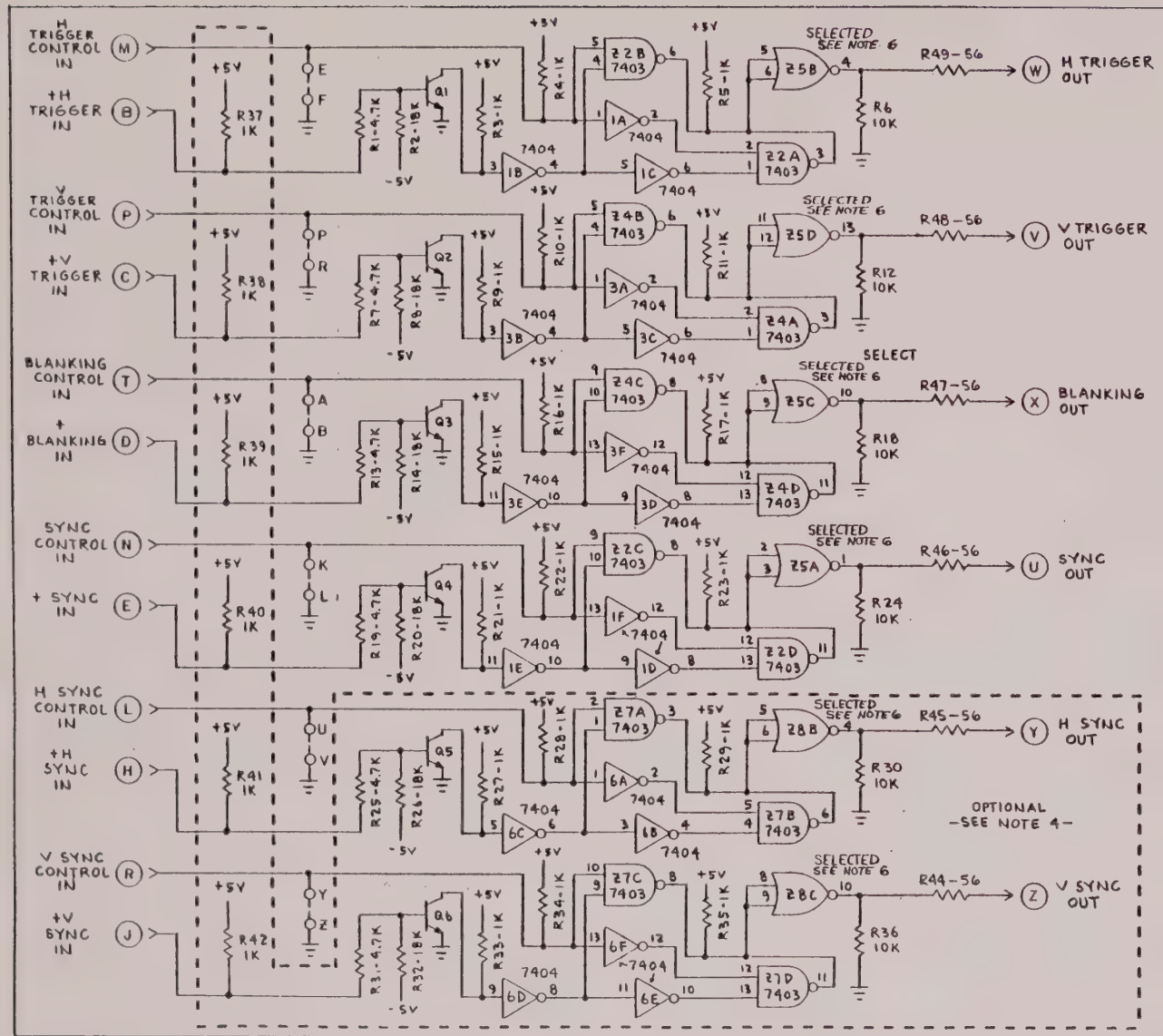
NO. HOLES/BOARD = 280

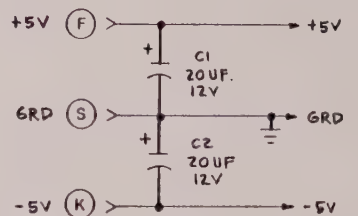
NOTES:
1) ALL TRANSISTORS = 2N5134.
2) ALL RESISTORS = 1/4W, ± 10% TOL.
3) C3 THRU C10 = 0.1UF, 10V.
4) JUMPERS A-B, E-F, K-L, P-R, U-V, Y-Z ARE USED TO SELECT PROPER POLARITY OF OUTPUT PULSES:
JUMPER INSTALLED — NEGATIVE PULSES ONLY.
JUMPER NOT INSTALLED — POSITIVE PULSES OR REMOTE CONTROL.

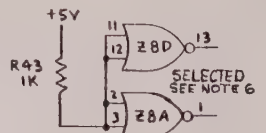
POSITION 12C 2118 TTL PULSE OUTPUT (Group 5)

MODEL 2501-H
WIRING INTERCONNECTIONS

CONNECTOR PIN	FUNCTION	DESTINATION
Z	V SYNC OUT . . .	(REAR PANEL, J16, V SYNC)
Y	H SYNC OUT . . .	(REAR PANEL, J15, H SYNC)
X	BLANK OUT	(REAR PANEL, J13, BLANKING)
W	H TRIGGER OUT . .	(REAR PANEL, J11, H TRIGGER)
V	V TRIGGER OUT . .	(REAR PANEL, J12, V TRIGGER)
U	SYNC OUT	(REAR PANEL, J14, SYNC)
T	BLANK CONTROL . .	(REAR PANEL, S103, BLANKING)
S	GROUND	(GROUND BUSS)
R	V SYNC CONTROL . .	(REAR PANEL, S106, V SYNC)
P	V TRIGGER CONTROL.	(REAR PANEL, S102, V TRIGGER)
N	SYNC CONTROL . .	(REAR PANEL, S104, SYNC)
M	H TRIGGER CONTROL.	(REAR PANEL, S101, H TRIGGER)
L	H SYNC CONTROL . .	(REAR PANEL, S105, H SYNC)
K	-5v.	(-5v. BUSS)(POWER REGULATOR, PIN A)
J	+V SYNC IN	(uP INTERFACE (P1), PIN J)
H	+H SYNC IN	(uP INTERFACE (P1), PIN 2)
F	+5v.	(+5v. BUSS)(POWER REGULATOR, PIN C)
E	+SYNC IN	(TTL PULSE OUTPUT, PIN E)(VIDEO CONTROL, PIN A)(uP INTERFACE (P1), PIN 3)
D	+BLANK IN	(TTL PULSE OUTPUT, PIN D)(RESOLUTION (7C,9C), PIN R)(CHARACTER, PIN Z)(CLOCKED BAR/DOT, PIN J)(RESOLUTION CONTROL, PIN C)(uP INTERFACE (P1), PIN 6)
C	+V TRIGGER IN . .	(uP INTERFACE (P1), PIN 8)
B	+H TRIGGER IN . .	(uP INTERFACE (P1), PIN B)
A	--	
	GROUND	(REAR PANEL, J16, V SYNC GROUND)

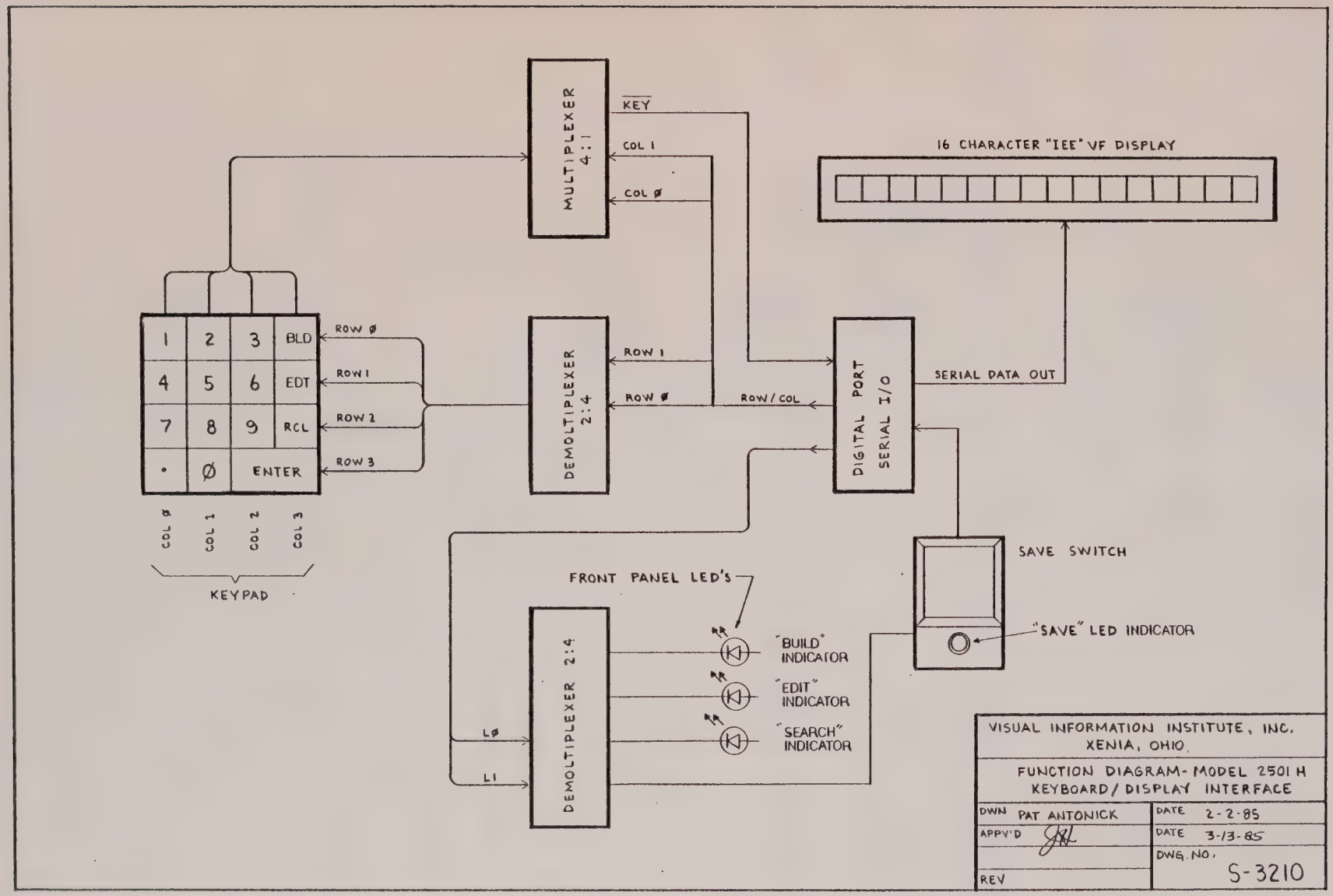






NOTES:
1) ALL TRANSISTORS = 2N5134.
2) ALL RESISTORS = 1/4W, ± 10% TOL.
3) C3 THRU C10 = 0.1 UF, 10V. (NOT SHOWN).
4) FOR OPTIONAL PARTS, PER GROUP LISTING, RERER TO INDIVIDUAL GROUP ASS'Y. DW6S. L-2118 (GRP 1 THRU 25)
5) JUMPERS A-B, E-F, K-L, P-R, U-V, Y-Z ARE USED TO SELECT PROPER POLARITY OF OUTPUT PULSES:
JUMPER INSTALLED – NEGATIVE PULSES ONLY
JUMPER NOT INSTALLED – POSITIVE PULSES OR REMOTE CONTROL.
6) FOR Z5 & Z8 SELECTION SEE PL-2118 SHT. 3

VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
TTL PULSE OUTPUT	
DRN. PAT ANTONICK	DATE 1-22-82
APPV'L. L.R. Button	DATE 2-11-82
P.C. ART REV. C (3-83)	DWG. NO. S-2118
REV. 4-26-84	


MULTIPLEXER 4:1
KEY
COL 1
COL Ø
16 CHARACTER "IEE" VF DISPLAY
1 2 3 BLD
4 5 6 EDT
7 8 9 RCL
• Ø ENTER
ROW Ø
ROW 1
ROW 2
ROW 3
COL Ø
COL 1
COL 2
COL 3
KEYPAD
DEMOLTIPLEXER 2:4
ROW 1
ROW Ø
ROW/COL
DIGITAL PORT SERIAL I/O
SERIAL DATA OUT
SAVE SWITCH
"SAVE" LED INDICATOR
FRONT PANEL LED'S
DEMOLTIPLEXER 2:4
LØ
L1
"BUILD" INDICATOR
"EDIT" INDICATOR
"SEARCH" INDICATOR
VISUAL INFORMATION INSTITUTE, INC.
XENIA, OHIO
FUNCTION DIAGRAM- MODEL 2501 H
KEYBOARD/DISPLAY INTERFACE
DWN PAT ANTONICK
DATE 2-2-85
APPV'D
DATE 3-13-85
DWG. NO. S-3210
REV

KEYBOARD INTERFACE
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST — PL-2194
ARTWORK REV. A (3/84) — 11/30/84 — SHT 1 OF 2

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/ TYPE	QTY	MFR	Vii DWG. NO.
REF.	SCHEMATIC			Vii	DS-2194
REF.	COMPONENT LAYOUT (ASS'Y)			Vii	DL-2194
REF.	PC ARTWORK (COND. SIDE)			Vii	DB-2194
REF.	PC ARTWORK (COMP. SIDE)			Vii	DF-NONE
REF.	DRILL DWG.			Vii	DD-2194
R1 - R4	Resistor, Fixed	470 ohms	4	BAS	A-1450
R5-R12	Resistor, Fixed	3.3K ohms	8	BAS	A-1450
RN1	Resistor Network-SIP	6 pin (10K)	1	BAS	A-1873
C1	Capacitor	1uf, 50v	1	BAS	
C5, C6	Capacitor	0.1uf, 10v	2	BAS	A-1455
J1	Connector (header)	40 pin (20 dbl row)	1	AP Prod.	929836-01
J2	Connector (header)	26 pin (13 dbl row)	1	AP Prod.	929836-01
J3, J4	Connector	6 pin	2	Berg	65801-006
J3, J4	Sticks Header	Single Line, (6 position)	2	AP Prod.	929834-01
- -	I.C. Socket	16 pin	2	BAS	A-1465
U3	I.C.	74LS139	1	BAS	
U4	I.C.	74LS153	1	BAS	
- -	Bus wire, jumper	#22 Awg Solid	14	BAS	

KEYBOARD INTERFACE
PRINTED CIRCUIT BOARD ASSEMBLY

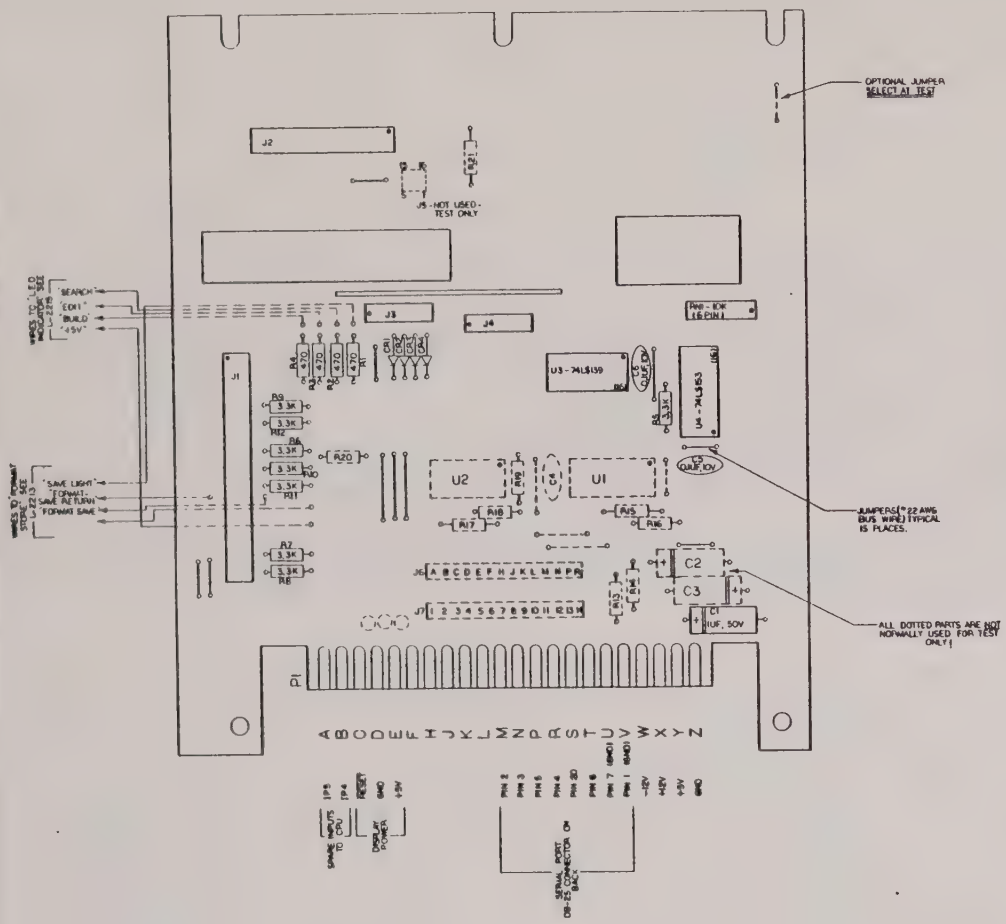
PARTS LIST
ARTWORK REV. A (3/84)   11/30/84   PL-2194
SHT 2 OF 2

* *

NOTE: The following optional parts are not normally used (for test only).

* *

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/ TYPE	QTY	MFR	Vii DWG. NO.
CR1-CR4	Diode	1N4154	4	BAS	A-1797
R13,14,15, 16,20,21	Resistor, Fixed	3.3K ohms	6	BAS	A-1450
R17,18,19	Resistor, Fixed	39K ohms	3	BAS	A-1450
C2, C3	Capacitor	1uf, 25v	2	BAS	A-1458
C4	Capacitor	0.1uf, 10v	1	BAS	A-1455
J5	Connector (header)	4 pin (2 dbl row)	1	AP Prod.	929836-01
J6, J7	Connector (header)	14 pin (single row)	2	AP Prod.	929834-01
- -	I.C. Socket	14 pin	2	BAS	A-1465
U1	I.C.	1488	1	BAS	
U2	I.C.	1489	1	BAS	
- -	Stake pins		3	Keystone	1575-2
- -	Scotcal labels	"A thru R" & "1 thru 14"	2	Vii	DB-2194
- -	Bus wire, jumpers	#22 Awg Solid	4	BAS	

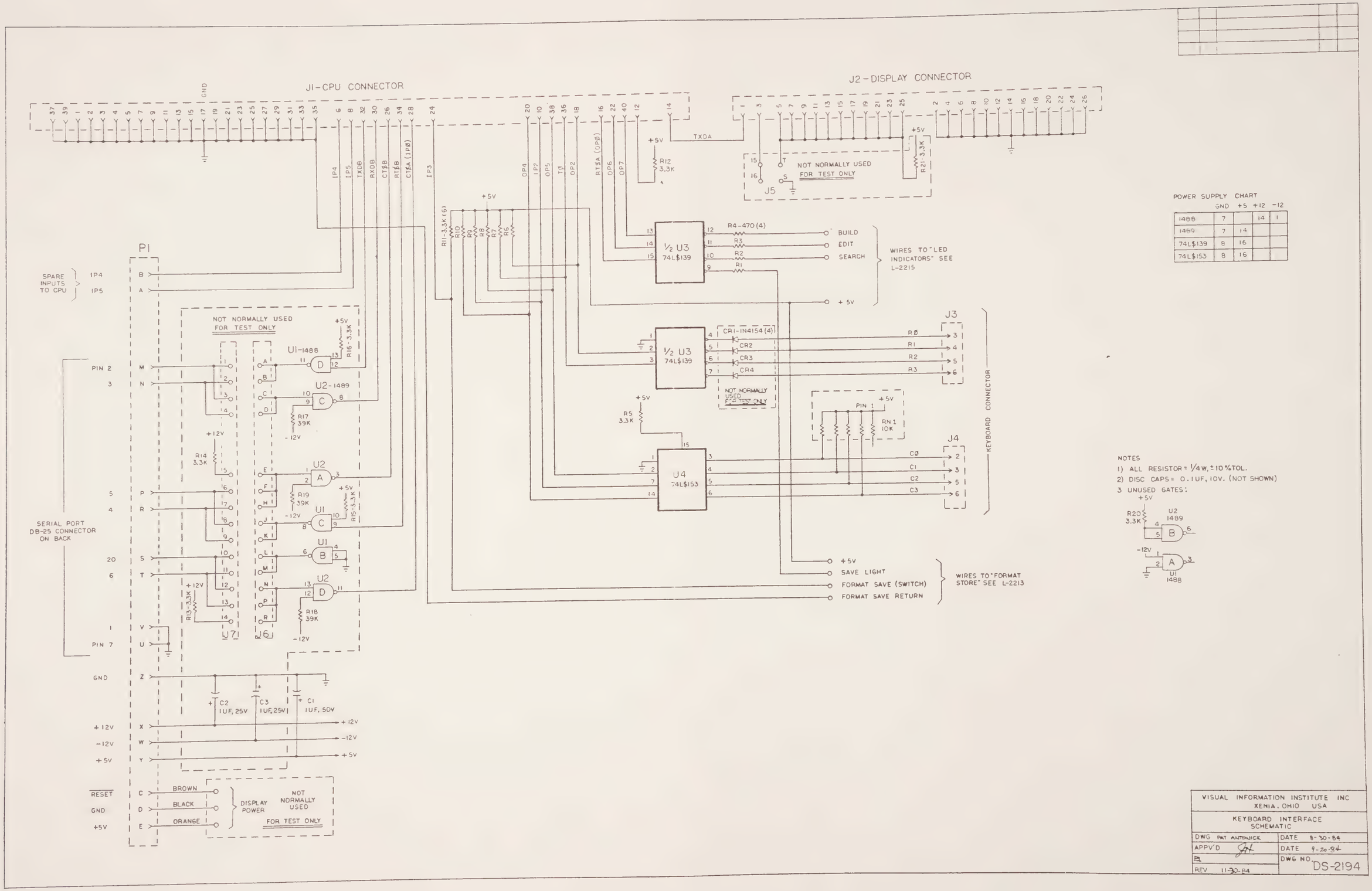


REFERENCE DESIGNATOR CHART

REF. DESIG	LAST	NOT
CR	CR4	
C	C6	
R	R20	
RN	RN1	
J	J7	
U	U4	

NOTES:
1) FOR PARTS LIST SEE PL-2194
2) FOR SCHEMATIC SEE DS-2194
3) ALL RESISTORS-1/4W; ± 10% TOL.
4) ALL DIODES = IN4154

VISUAL INFORMATION INSTITUTE, INC XENIA, OHIO	
KEYBOARD INTERFACE COMPONENT LAYOUT	
DRN WARNER	DATE 11-30-84
APP'D	DATE 1-22-85
PC ART REV. A 13-84	DWG NO DL-2194
REV	



POWER SUPPLY CHART

	GND	+5	+12	-12
1488	7		14	1
1489	7	14		
74L$139	8	16		
74L$153	8	16		

NOTES
1) ALL RESISTOR = 1/4W, ±10% TOL.
2) DISC CAPS = 0.1UF, 10V. (NOT SHOWN)
3 UNUSED GATES:

VISUAL INFORMATION INSTITUTE INC
XENIA, OHIO USA

KEYBOARD INTERFACE SCHEMATIC

DWG PAT ANTONICK	DATE 8-30-84
APPV'D	DATE 9-20-84
	DWG NO. DS-2194
REV 11-30-84	

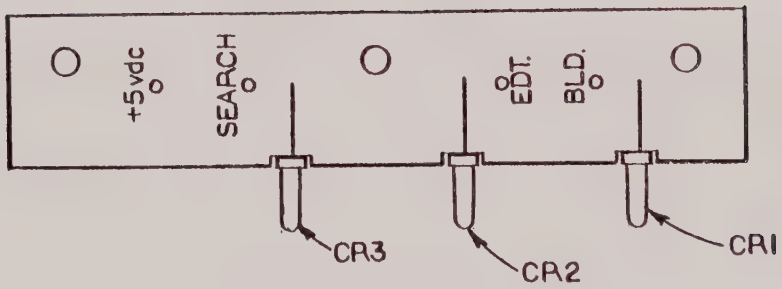
LED INDICATOR
PRINTED CIRCUIT BOARD ASSEMBLY

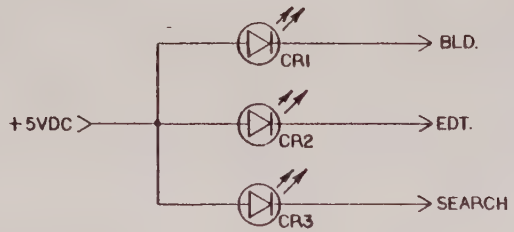
PARTS LIST PL-2215

ARTWORK REV. A (2/84) 12/10/84 SHT 1 OF 1

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/ TYPE	QTY	MFR	Vii DWG.NO.
REF.	PC ASSEMBLY			Vii	L-2215
REF.	PC ARTWORK (COND. SIDE)			Vii	AB-2215
REF.	PC ARTWORK (COMP. SIDE)			Vii	AF-2215
REF.	SCHEMATIC			Vii	S-2215
CR1,2,3	Diode, light emitting	MV5094	3	BAS	

LED INDICATOR | 2-84 REV. A | DWG NO. L-2215 | (GROUP 0) | DATE 12-10-84





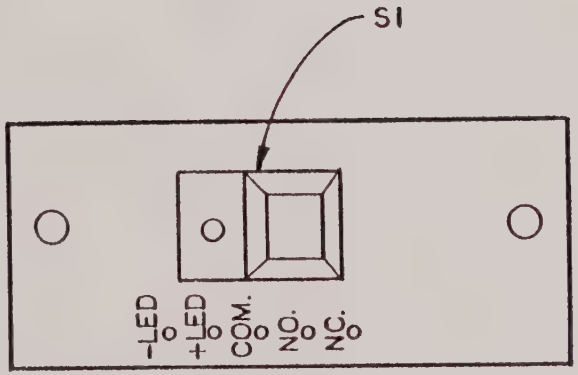
VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
LED INDICATOR	
DRN D.W.	DATE 12-10-84
APPV'D [illegible]	DATE 12-13-84
P.C. ART REV A (2-84)	DWG. NO. S-2215
REV.	

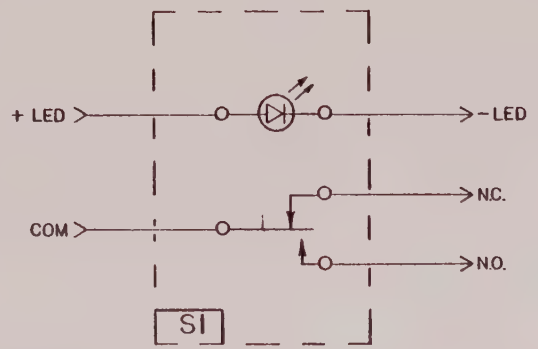
FORMAT STORE
PRINTED CIRCUIT BOARD ASSEMBLY

PARTS LIST PL-2213

ARTWORK REV. A (2/84) 12/10/84 SHT 1 OF 1

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/ TYPE	QTY	MFR	Vii DWG.NO.
REF.	PC ASSEMBLY			Vii	L-2213
REF.	PC ARTWORK (COND. SIDE)			Vii	AB-2213
REF.	PC ARTWORK (COMP. SIDE)			Vii	AF-2213
REF.	SCHEMATIC			Vii	S-2213
S1	Switch, key	P.C. type	1	BAS	A-2291


S1
-LED
+LED
COM.
NO
NC



VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
FORMAT STORE	
DRN. D.W.	DATE 12-10-84
APPV'D [illegible]	DATE 12-13-84
P.C. REV. A (2-84)	DWG NO. S-2213
REV.	

HEAT SINK FILTER ASSEMBLY
PRINTED CIRCUIT BOARD ASSEMBLY

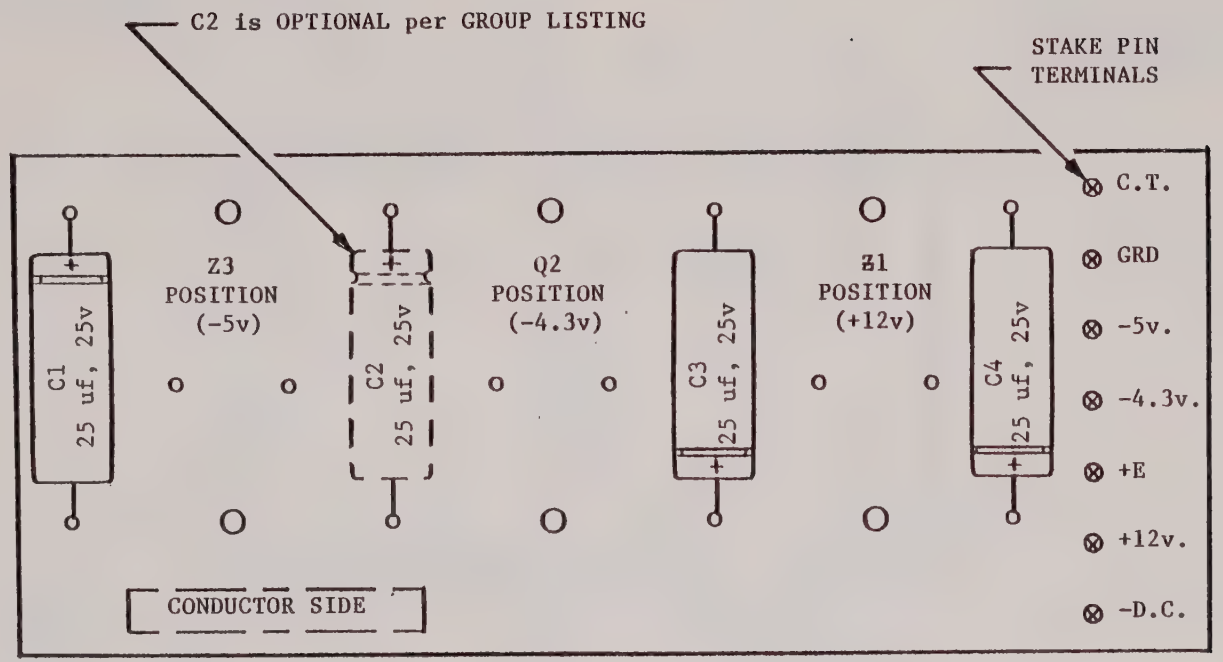
PARTS LIST PL-2115

ARTWORK REV. C (9/83) 10/13/83 SHT 1 of 1

DESCRIPTION	VALUE/TYPE	QTY/GROUP 1	2	3	4	MFR.	Vii DWG.NO.
Assembly		x	x	x	x	Vii	L-2115
Schematic		x	x	x	x	Vii	S-2115
PCB - Section A		1	1	1	1	Vii	CB-2115A
PCB - Section B		1	1	1	1	Vii	CB-2115B
PCB - Section C		1	1	1	1	Vii	CB-2115C
Bracket, Heat Sink		1	1	1	1	Vii	B-1618
Diode, Power		4	4	4	4	BAS	A-1851
Transistor, NPN	2N3055	1	1	1	1	BAS	A-1836
Transistor, PNP	MJ2955	1	1	x	x	BAS	A-1833
Voltage Reg. +12v	LM340K-12	1	1	1	1	BAS	A-1774
Voltage Reg. +8v	LM340K-8	1	x	x	1	BAS	A-1774
Voltage Reg. -5v	LM320K-5	1	1	1	1	BAS	A-1775
Capacitor	25uf, 25v	6	5	4	5	BAS	A-1458
Capacitor	2200uf, 35v	1	1	1	1	BAS	
Capacitor	3300uf, 35v	1	1	1	1	BAS	
Capacitor	10000uf,35v	1	1	1	1	BAS	
Mounting Kit	DO-4	4	4	4	4	BAS	A-1876
Insulator, Mica	TO-3	5	4	3	4	BAS	A-1765
Insulator, Molded	TO-3	5	4	3	4	BAS	A-1721P2
Thermal Compound		AR	AR	AR	AR	BAS	
Spacer		10	10	10	10	BAS	A-1877
Screw, BH	#4-40x3/16	2	2	2	2	BAS	
Screw, BH	#4-40x3/4	10	10	10	10	BAS	
Washer, Plain	#4	x	2	4	2	BAS	
Washer, Lock	#4	12	12	12	12	BAS	
Nut, Hexagon	#4-40 UNC	10	10	10	10	BAS	
Wire, stranded	#18 Awg	AR	AR	AR	AR	BAS	

HEATSINK FILTER - SECTION A (9-83) REV. C DWG. NO. L-2115A PARTS LIST

10-13-83



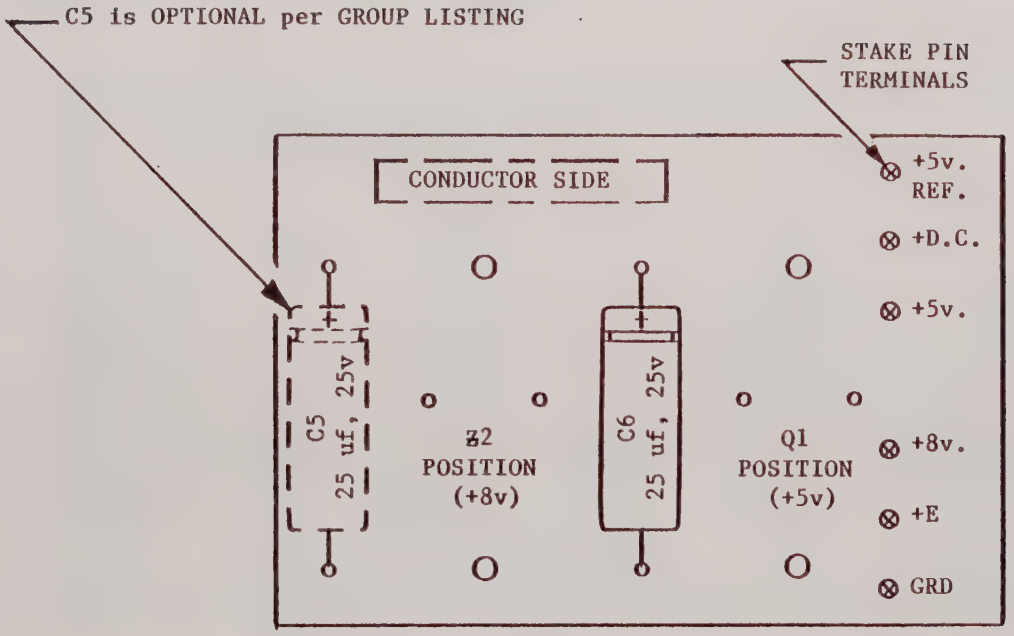
NOTES:

1. Install Capacitors (C1, C2, C3 & C4) and STAKE PIN TERMINALS (7 Req'd) to the Conductor Side of the P. C. Board.
2. Power Regulators (Z1, Q2 & Z3) are installed at final assembly. See Dwg. No. L-2115.

NO.	HOLES/BOARD
GROUP 1	= 15
GROUP 2	= 15
GROUP 3	= 13

HEATSINK FILTER - SECTION B (9-83) REV. C DWG. NO. L-2115B PARTS LIST

10-13-83



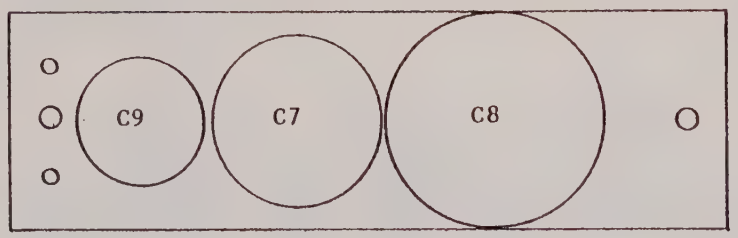
NOTES:

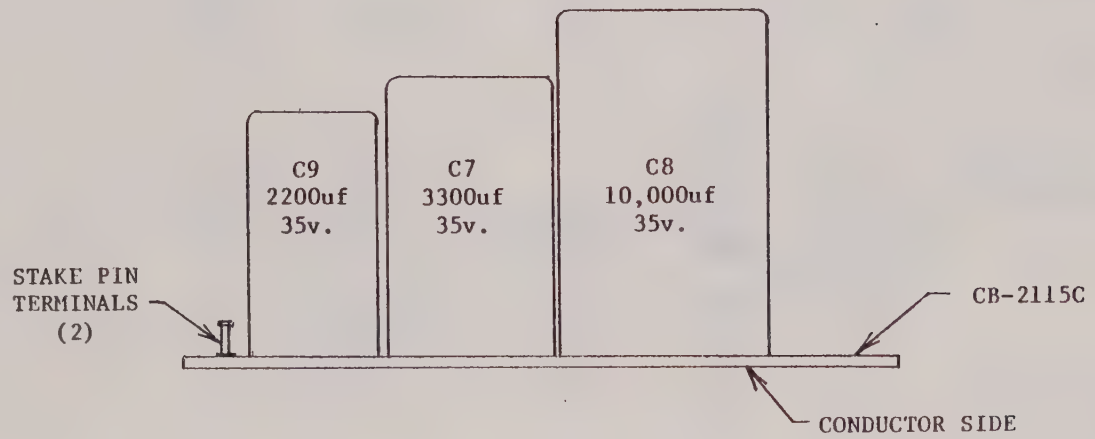
1. Install Capacitors (C5 & C6) and STAKE PIN TERMINALS (6 Req'd) to the Conductor Side of the P.C. Board.
2. Power Regulators (Q1 & Z2) are installed at final Assembly. See Dwg. No. L-2115

NO. HOLES/BOARD	
GROUP 1 =	10
GROUP 2 =	8
GROUP 3 =	8

HEATSINK FILTER - SECTION C (9-83) REV. C DWG. NO. L-2115C PARTS LIST

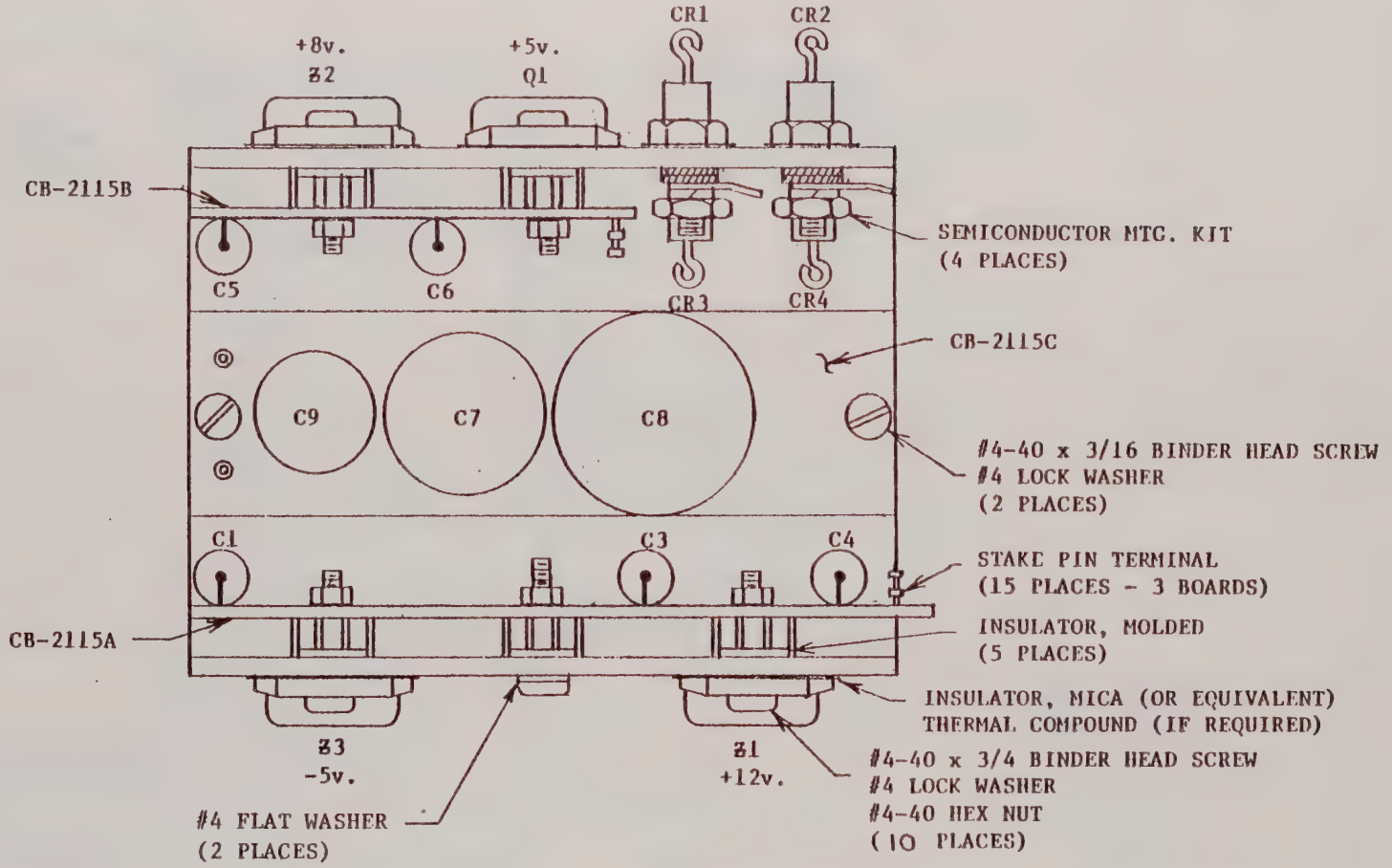
10-13-83

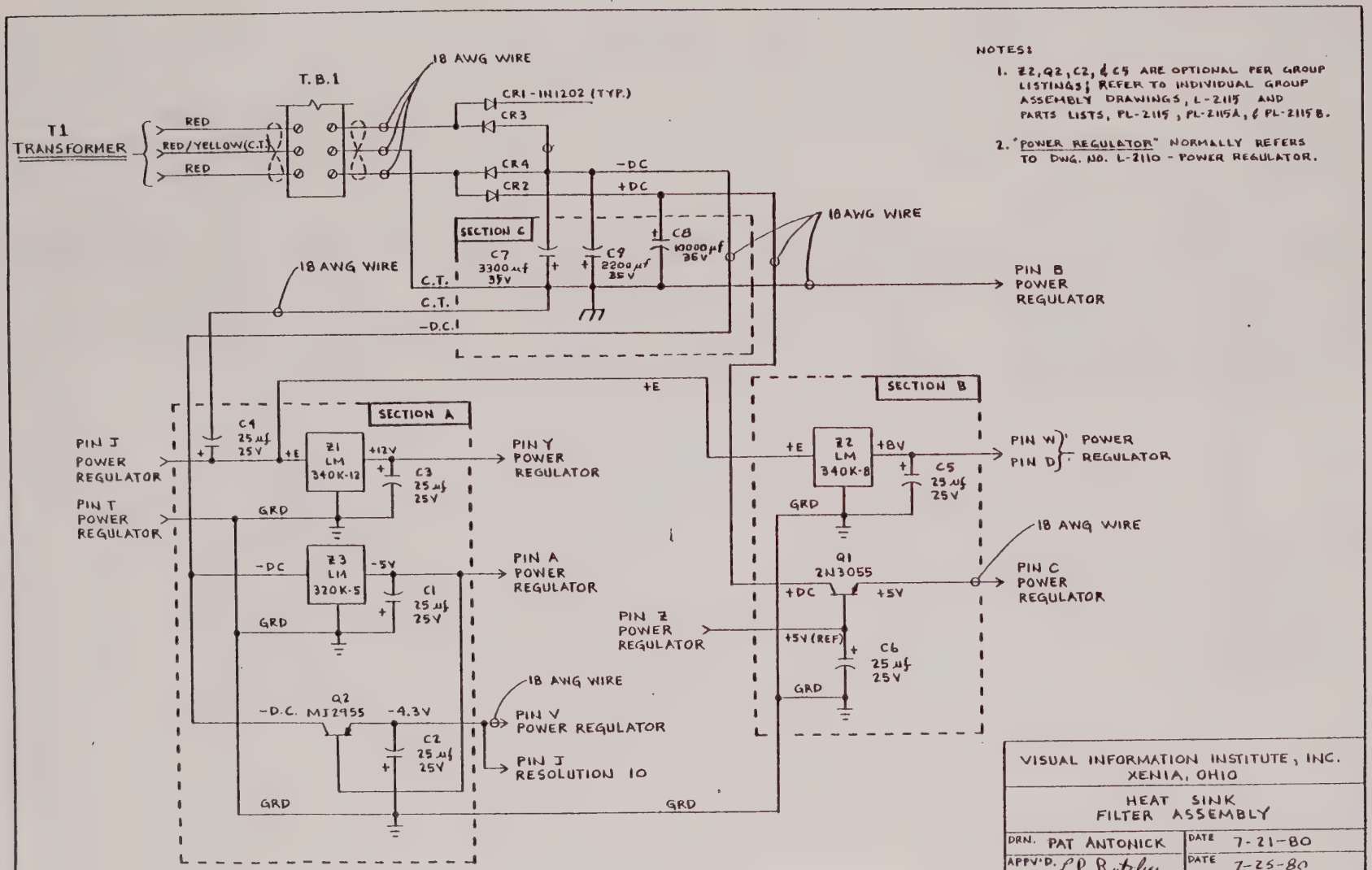




NO. HOLES/BOARD = 8

HEATSINK FILTER ASSEMBLY REV. C (9-83) DWG. NO. L-2115 (GROUP 4) PARTS LIST 10-13-83





VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
HEAT SINK FILTER ASSEMBLY	
DRN. PAT ANTONICK	DATE 7-21-80
APPV'D. L.R. Butcher	DATE 7-25-80
P.C. ART. REV. C (9-83)	DWG. NO S-2115
REV. 10-13-83	

REPLACEABLE PARTS LIST

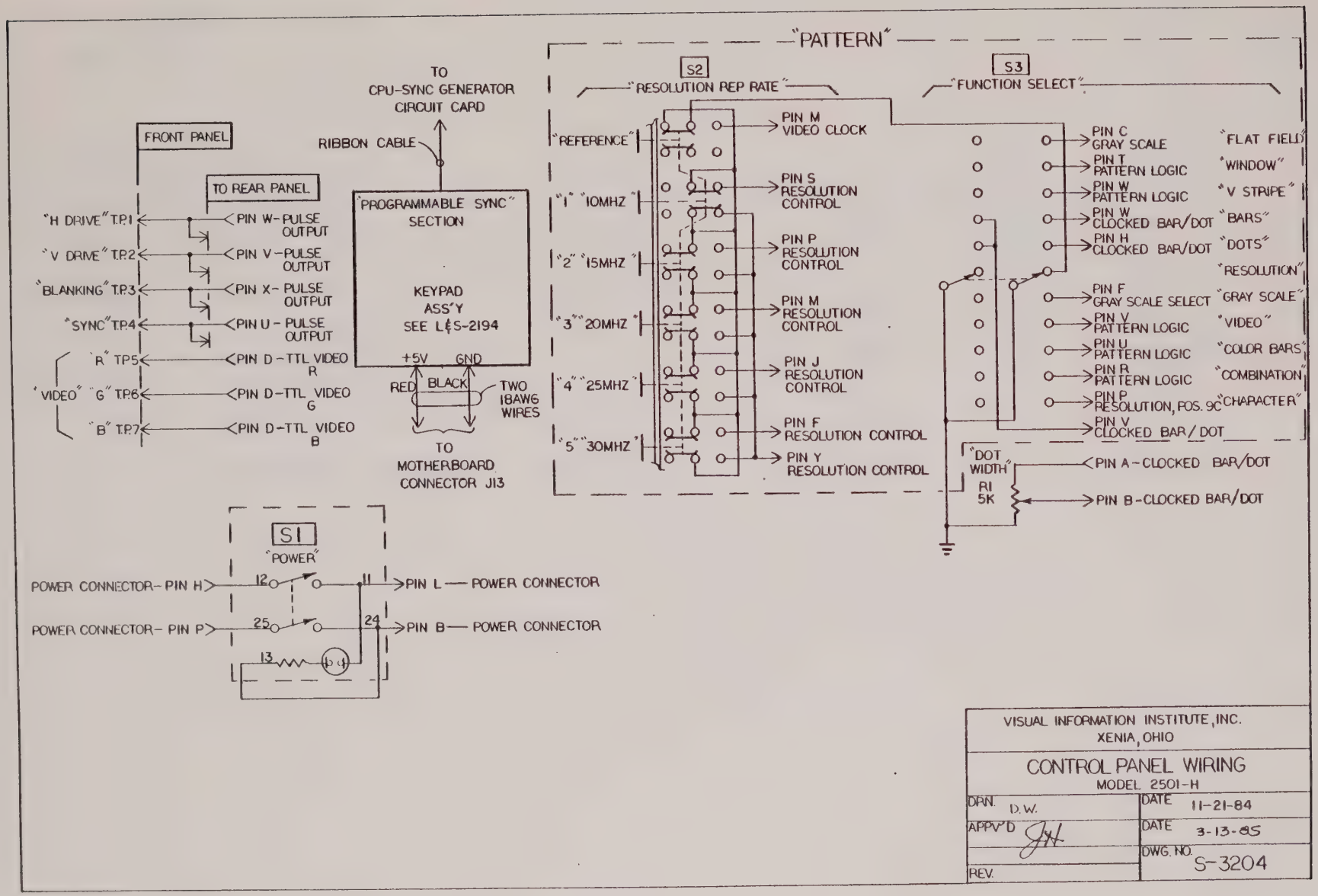
CONTROL PANEL WIRING

MODEL 2501-H

PL-3204

11/21/84

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/TYPE	QTY	MFR	Vii DWG.NO.	REFERENCE NUMBER
	Knob, Pointer	Medium, Skirted	1	BAS	A-1770	70-3-2G
R1	Resistor, Variable	5K ohm	1	BAS	A-1138 P4	RV6NAYSD502A
S1	Switch, Rocker	110v AC	1	BAS	A-2210-1	2600R11E
S2	6 Pushbutton Switch	Group 0	1	Vii	L-2224	
S3	Switch Assembly	2 Deck Rotary 2 Pole, 11 Position	1	BAS	A-1131P1	T-215
TP1 - TP7	Test Points	Red/Tip Jack	7	BAS	A-1822	1505
	Digital Display	Flip Module 1 x 16 seg.	1	IEE		037000-13-016
	Flip Filter	Green	1	IEE		26542-07
	Keypad	Full travel membrane	1	Oak		5-64951-052
	Key Caps	Double Wide	1	Cherry		028-0356
	Key Caps	Single	12	Cherry		028-1755



VISUAL INFORMATION INSTITUTE, INC.
XENIA, OHIO

CONTROL PANEL WIRING

MODEL 2501-H

DRN. D.W.	DATE 11-21-84
APP'V'D J.H.	DATE 3-13-85
REV.	DWG. NO. S-3204

REPLACEABLE PARTS LIST

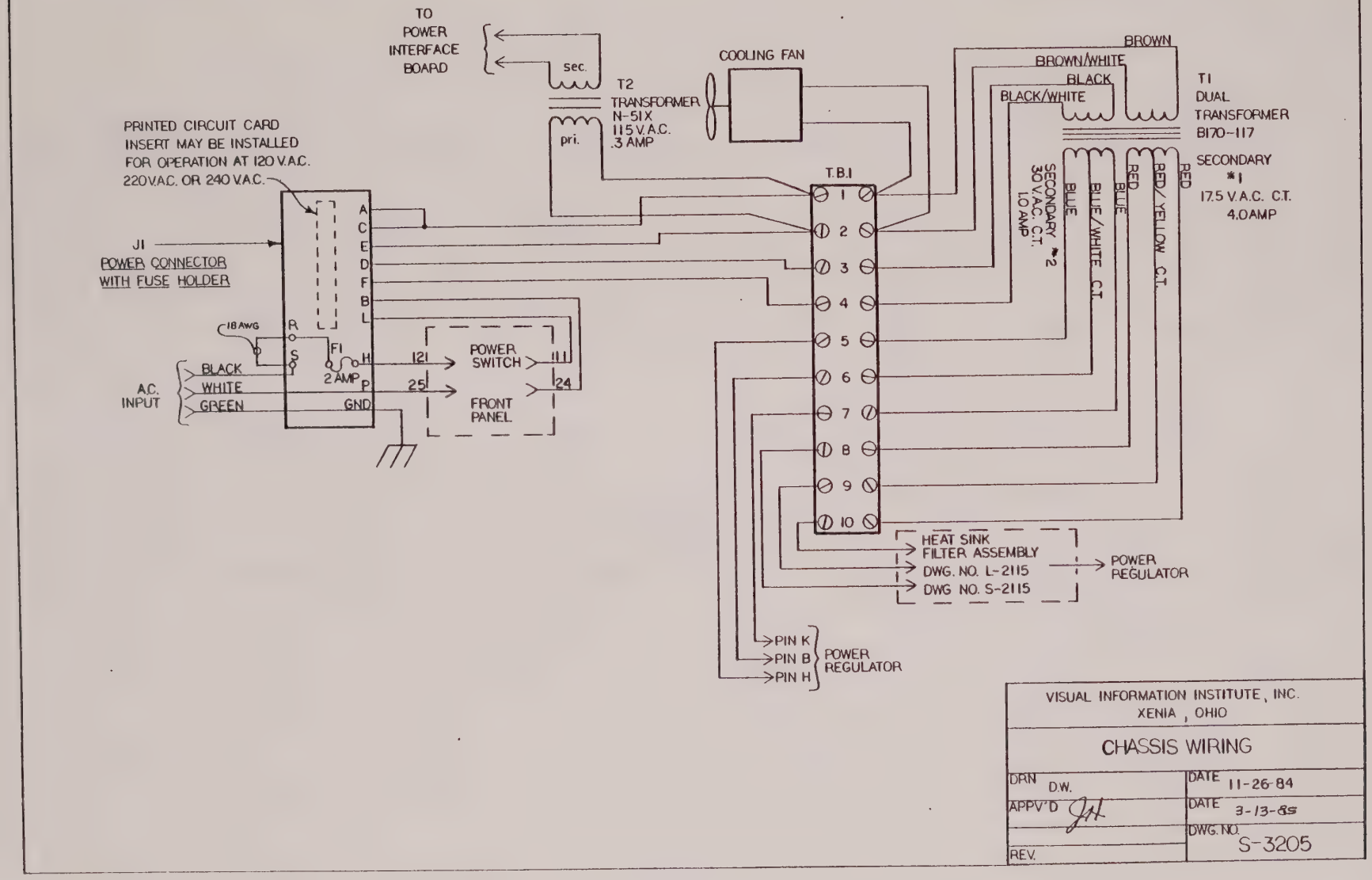
PL-3205

CHASSIS WIRING

MODEL 2501-H

11/26/84

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/TYPE	QTY	MFR.	Vii DWG.NO.	REFERENCE NUMBER
J1	Connector, Power	Non-filtered	1	BAS	A-1791A A-1791B	6J1
T.B.1	Terminal Block	10 contacts	1	BAS	A-1744	10-140
F1	Fuse, Slo-blo	2 amp	1	BAS	A-1743	MDL-2
--	Fan, Cooling		1	BAS	A-1745	SU2A1/028267
--	Guard, Finger		1	BAS	A-1746	476-143
T1	Transformer, Dual	17.5VAC C.T. 4A 30VAC C.T. 1A	1 1	BAS BAS	B-1723	B170-117
T2	Transformer, Isolation	115VAC .3A	1	BAS		N51X



VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
CHASSIS WIRING	
DRN D.W.	DATE 11-26-84
APPV'D	DATE 3-13-85
REV.	DWG. NO. S-3205

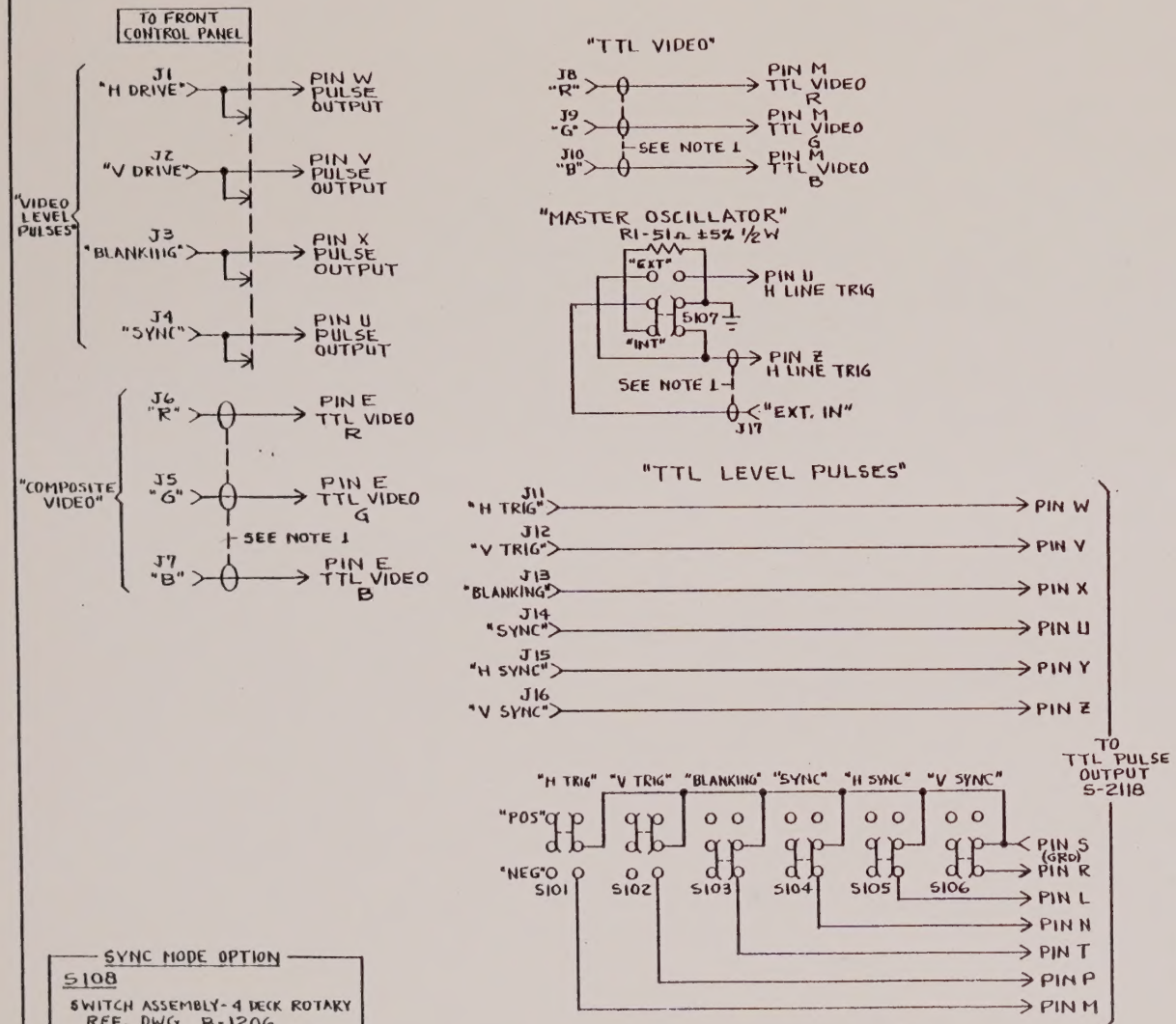
REPLACEABLE PARTS LIST

REAR CONNECTOR PANEL WIRING

PL-3070

9/15/83

REFERENCE DESIGNATOR	DESCRIPTION	VALUE/TYPE	QTY	MFR	Vii DWG.NO.	REFERENCE NUMBER
J1 thru J4 J11 thru J16	Connector, Coaxial	BNC	10	BAS	A-1787	UG-1094/U
J5 thru J10, J17	Connector, Coaxial Isolated	BNC	7	BAS	A-1788	31-10
S101 thru S107	Switch, Slide	DPDT	7	Vii	A-1794-P1	1227
S108	Switch Assembly	4 deck rotary	1	Vii	B-1206	
R1	Resistor, Fixed	51 ohms, 1/2w	1	BAS	A-1446	

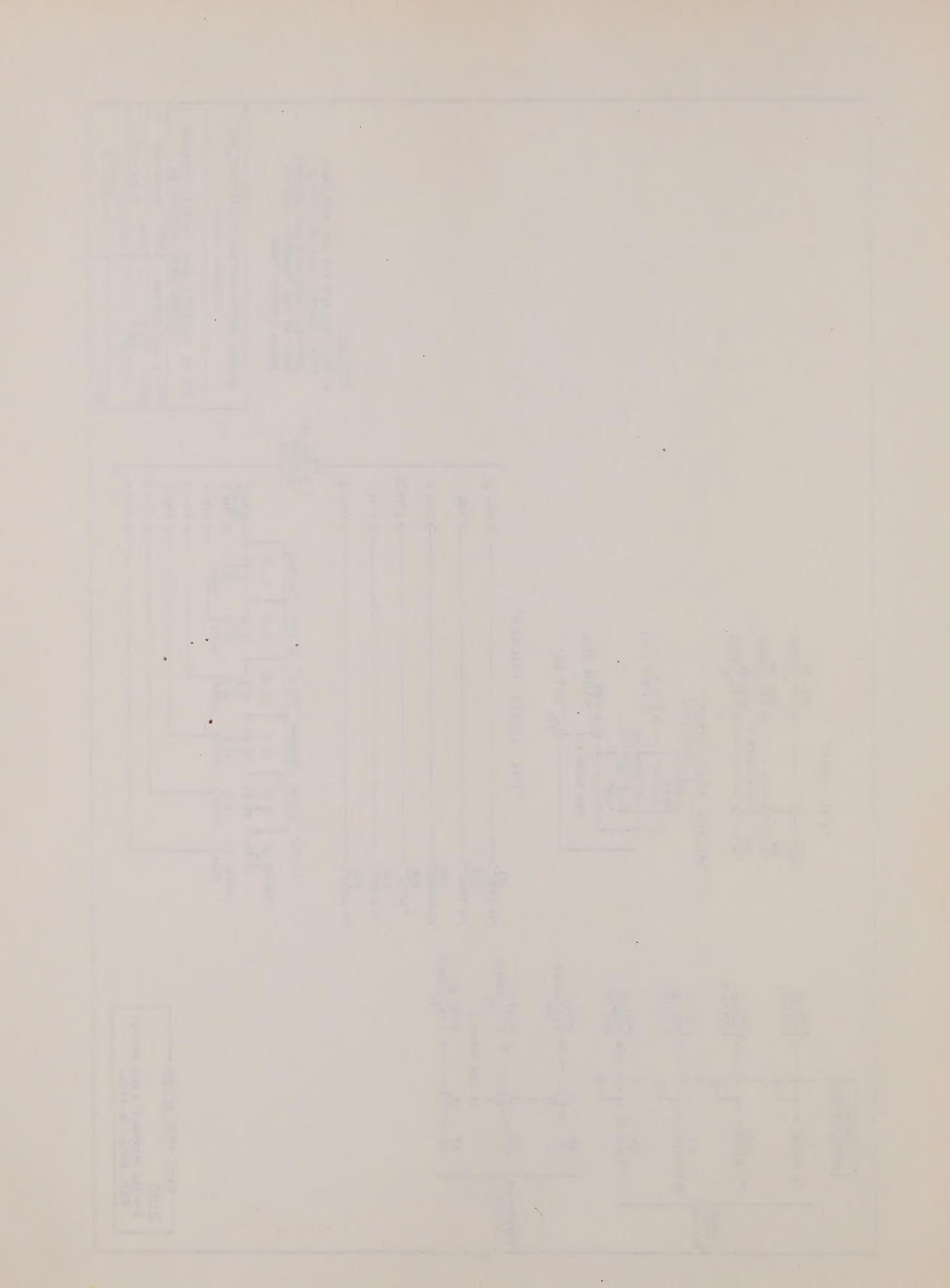


SYNC MODE OPTION

S108

SWITCH ASSEMBLY-4 DECK ROTARY
REF. DWG B-1206

NOTES~

1. J5, 6, 7, 8, 9, 10 & 17 ARE INSULATED FROM PANEL. COAXIAL CABLE SHIELDS INDICATED ARE GROUNDED ONLY AT THE PRINTED-CIRCUIT BOARD CONNECTORS.

VISUAL INFORMATION INSTITUTE, INC. XENIA, OHIO	
REAR CONNECTOR PANEL WIRING PRODUCTION SERIES H	
DRN L.W. AUSTIN	DATE 9-15-83
APP'D JL	DATE 9-23-83
	DWG NO. S-3070
REV.